JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.Tech. (VLSI/ VLSI DESIGN/VLSI SYSTEM DESIGN)

COURSE STRUCTURE AND SYLLABUS

I Year – I Semester

Category	Course Title	Int. marks	Ext. marks	L	P	C
Core Course I	VLSI Technology	25	75	4	--	4
Core Course II	CMOS Analog Integrated Circuit Design	25	75	4	--	4
Core Course III	CMOS Digital Integrated Circuit Design	25	75	4	--	4
Core Elective I	Digital System Design Hardware Software Co-Design CPLD and FPGA Architectures and Applications	25	75	4	--	4
Core Elective II	Algorithms for VLSI Design Automation Embedded System Design Device Modeling	25	75	4	--	4
Open Elective I	Soft Computing Techniques Image and Video processing Software Defined Radio	25	75	4	--	4
Laboratory I	VLSI Laboratory – I	25	75	--	4	2
Seminar I	Seminar	50	--	--	4	2
Total Credits				**24**	**8**	**28**

I Year – II Semester

Category	Course Title	Int. marks	Ext. marks	L	P	C
Core Course IV	Low Power VLSI Design	25	75	4	--	4
Core Course V	Design for Testability	25	75	4	--	4
Core Course VI	CMOS Mixed Signal Circuit Design	25	75	4	--	4
Core Elective III	VLSI and DSP Architectures Full custom IC Design Hardware Description Language	25	75	4	--	4
Core Elective IV	Optimization Techniques in VLSI Design System On Chip Architecture Semiconductor Memory Design and Testing	25	75	4	--	4
Open Elective II	Scripting Languages Coding Theory and Techniques Adhoc Wireless Networks	25	75	4	--	4
Laboratory II	VLSI Laboratory – II	25	75	--	4	2
Seminar II	Seminar	50	--	--	4	2
Total Credits				**24**	**8**	**28**

II Year - I Semester

Course Title	Int. marks	Ext. marks	L	P	C
Comprehensive Viva-Voce	--	100	--	--	4
Project work Review I	50	--	--	24	12
Total Credits			--	24	**16**

II Year - II Semester

Course Title	Int. marks	Ext. marks	L	P	C
Project work Review II	50	--	--	8	4
Project Evaluation (Viva-Voce)	--	150	--	16	12
Total Credits			**--**	**24**	**16**

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M. Tech – I Year – I Sem. (VLSI/VLSI Design/VLSI System Design)

VLSI TECHNOLOGY

UNIT –I:

Review of Microelectronics and Introduction to MOS Technologies:

MOS, CMOS, BiCMOS Technology. Basic Electrical Properties of MOS, CMOS & BiCMOS Circuits: Ids – Vds relationships, Threshold Voltage VT, Gm, Gds and ωo, Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT –II:

Layout Design and Tools:

Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools.

Logic Gates & Layouts:

Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

UNIT –III:

Overview of semiconductor industry, Stages of Manufacturing, Process and product trends, Crystal growth, Basic wafer fabrication operations, process yields, Semiconductor material preparation, Basic wafer fabrication operations, Yield measurement, Contamination sources, Clean room construction, Oxidation and Photolithography, Doping and Depositions, Metallization.Ten step patterning process, Photoresists, physical properties of photoresists, Storage and control of photoresists, photo masking process, Hard bake, develop inspect, Dry etching Wet etching, resist stripping

UNIT –IV

Doping and depositions: Diffusion process steps, deposition, Drive-in oxidation, Ion implantation-1, Ion implantation-2, CVD basics, CVD process steps, Low pressure CVD systems, Plasma enhanced CVD systems, Vapour phase epitoxy, molecular beam epitaxy.

UNIT –V

Design rules and Scaling, BICMOS ICs: Choice of transistor types, pnp transistors, Resistors, capacitors,

Packaging: Chip characteristics, package functions, package operations

TEXT BOOKS:

1. Peter Van Zant, Microchip fabrication, McGraw Hill, 1997.
2. C.Y. Chang and S.M. Sze, ULSI technology, McGraw Hill, 2000

REFERENCE BOOKS:

1. Micro Electronics circuits Analysis and Design 2nd Edition, Muhammad H Rashid, CENAGE Learning2011.
2. Eugene D. Fabricius, Introduction to VLSI design, McGraw Hill, 1999
3. Wani-Kai Chen (editor), The VLSI Hand book, CRI/IEEE press, 2000
4. S.K. Gandhi, VLSI Fabrication principles, John Wiley and Sons, NY, 1994

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CMOS ANALOG INTEGRATED CIRCUIT DESIGN

UNIT -I:

MOS Devices and Modeling

The MOS Transistor, Passive Components- Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

UNIT -II:

Analog CMOS Sub-Circuits:

MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT -III

CMOS Amplifiers:

Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

UNIT -IV

CMOS Operational Amplifiers:

Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power-Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OP Amp.

UNIT -V

Comparators:

Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

TEXT BOOKS:

CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.

Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition, 2010.

REFERENCE BOOKS:

Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edn, 2013.

Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition.

CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce, PHI.

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CMOS DIGITAL INTEGRATED CIRCUIT DESIGN

UNIT –I:
MOS Design:
Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

UNIT –II:
Combinational MOS Logic Circuits:
MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates , AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT –III:
Sequential MOS Logic Circuits:
Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flipflop.

UNIT –IV:
Dynamic Logic Circuits:
Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

UNIT –V:
Semiconductor Memories:
Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory- NOR flash and NAND flash.

TEXT BOOKS:
1. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

REFERENCE BOOKS:
1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Digital Integrated Circuits – A Design Perspective, Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, 2nd Ed., PHI.

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DIGITAL SYSTEM DESIGN

(Core Elective –I)

UNIT -I:

Minimization and Transformation of Sequential Machines:

The Finite State Model – Capabilities and limitations of FSM – State equivalence and machine minimization – Simplification of incompletely specified machines.

Fundamental mode model – Flow table – State reduction – Minimal closed covers – Races, Cycles and Hazards.

UNIT -II:

Digital Design:

Digital Design Using ROMs, PALs and PLAs , BCD Adder, 32 – bit adder, State graphs for control circuits, Scoreboard and Controller, A shift and add multiplier, Array multiplier, Keypad Scanner, Binary divider.

UNIT -III:

SM Charts:

State machine charts, Derivation of SM Charts, Realization of SM Chart, Implementation of Binary Multiplier, dice game controller.

UNIT -IV:

Fault Modeling & Test Pattern Generation:

Logic Fault model – Fault detection & Redundancy- Fault equivalence and fault location –Fault dominance – Single stuck at fault model – Multiple stuck at fault models –Bridging fault model.

Fault diagnosis of combinational circuits by conventional methods – Path sensitization techniques, Boolean Difference method – Kohavi algorithm – Test algorithms – D algorithm, PODEM, Random testing, Transition count testing, Signature analysis and test bridging faults.

UNIT -V:

Fault Diagnosis in Sequential Circuits:

Circuit Test Approach, Transition Check Approach – State identification and fault detection experiment, Machine identification, Design of fault detection experiment

TEXT BOOKS:

1. Fundamentals of Logic Design – Charles H. Roth, 5th Ed., Cengage Learning.
2. Digital Systems Testing and Testable Design – Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman- John Wiley & Sons Inc.
3. Logic Design Theory – N. N. Biswas, PHI

REFERENCE BOOKS:

1. Switching and Finite Automata Theory – Z. Kohavi , 2nd Ed., 2001, TMH
2. Digital Design – Morris Mano, M.D.Ciletti, 4th Edition, PHI.
3. Digital Circuits and Logic Design – Samuel C. Lee , PHI

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M. Tech – I Year – I Sem. (VLSI/VLSI Design/VLSI System Design)

HARDWARE - SOFTWARE CO-DESIGN

(Core Elective –I)

UNIT –I:

Co- Design Issues:

Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

Co- Synthesis Algorithms:

Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT –II:

Prototyping and Emulation:

Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

Target Architectures:

Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT –III:

Compilation Techniques and Tools for Embedded Processor Architectures:

Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT –IV:

Design Specification and Verification:

Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

UNIT –V:

Languages for System – Level Specification and Design-I:

System – level specification, design representation for system level synthesis, system level specification languages,

Languages for System – Level Specification and Design-II:

Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system.

TEXT BOOKS:

1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf – 2009, Springer.
2. Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami, 2002, Kluwer Academic Publishers

REFERENCE BOOKS:

1. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont - 2010 – Springer

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M. Tech – I Year – I Sem. (VLSI/VLSI Design/VLSISystem Design)

CPLD AND FPGA ARCHITECURES AND APPLICATIONS

(Core Elective –I)

UNIT-I:

Introduction to Programmable Logic Devices:

Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

UNIT-II:

Field Programmable Gate Arrays:

Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs.

UNIT -III:

SRAM Programmable FPGAs:

Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 and XC4000 Architectures.

UNIT -IV:

Anti-Fuse Programmed FPGAs:

Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.

UNIT -V:

Design Applications:

General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

TEXT BOOKS:

1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition.
2. Digital Systems Design - Charles H. Roth Jr, Lizy Kurian John, Cengage Learning.

REFERENCE BOOKS:

1. Field Programmable Gate Arrays - John V. Oldfield, Richard C. Dorf, Wiley India.
2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/Samiha Mourad, Pearson Low Price Edition.
3. Digital Systems Design with FPGAs and CPLDs - Ian Grout, Elsevier, Newnes.
4. FPGA based System Design - Wayne Wolf, Prentice Hall Modern Semiconductor Design Series.

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M. Tech – I Year – I Sem. (VLSI/VLSI Design/VLSISystem Design)

ALGORITHMS FOR VLSI DESIGN AUTOMATION

(Core Elective –II)

UNIT I

PRELIMINARIES

Introduction to Design Methodologies, Design Automation tools, Algorithmic Graph Theory, Computational complexity, Tractable and Intractable problems.

UNIT II

GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION

Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu search, Genetic Algorithms.

UNIT III

LAYOUT COMPACTION, PLACEMENT, FLOORPLANNING AND ROUTING

Problems, Concepts and Algorithms.

MODELLING AND SIMULATION

Gate Level Modelling and Simulation, Switch level Modelling and Simulation.

UNIT IV

LOGIC SYNTHESIS AND VERIFICATION

Basic issues and Terminology, Binary-Decision diagrams, Two-Level logic Synthesis

HIGH-LEVEL SYNTHESIS

Hardware Models, Internal representation of the input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some aspects of Assignment problem, High-level Transformations.

UNIT V

PHYSICAL DESIGN AUTOMATION OF FPGAs

FPGA technologies, Physical Design cycle for FPGAs, partitioning and Routing for segmented and staggered Models.

PHYSICAL DESIGN AUTOMATION OF MCMs

MCM technologies, MCM physical design cycle, Partitioning, Placement - Chip Array based and Full Custom Approaches, Routing – Maze routing, Multiple stage routing, Topologic routing, Integrated Pin – Distribution and routing, Routing and Programmable MCMs.

TEXT BOOKS

1. Algorithms for VLSI Design Automation, S.H.Gerez, 1999, WILEY Student Edition, John wiley & Sons (Asia) Pvt. Ltd.
2. Algorithms for VLSI Physical Design Automation – Naveed Sherwani, 3rd Ed., 2005, Springer International Edition.

REFERENCE BOOKS

1. Computer Aided Logical Design with Emphasis on VLSI – Hill & Peterson, 1993, Wiley.
2. Modern VLSI Design:Systems on silicon – Wayne Wolf, 2nd ed., 1998, Pearson Education Asia.

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M. Tech – I Year – I Sem. (VLSI/VLSI Design/VLSI System Design)

EMBEDDED SYSTEMS DESIGN

(Core Elective –II)

UNIT -I:

Introduction to Embedded Systems

Definition of Embedded System, Embedded Systems Vs General Computing Systems, History of Embedded Systems, Classification, Major Application Areas, Purpose of Embedded Systems, Characteristics and Quality Attributes of Embedded Systems.

UNIT -II:

Typical Embedded System:

Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS), Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: Onboard and External Communication Interfaces.

UNIT -III:

Embedded Firmware:

Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer, Embedded Firmware Design Approaches and Development Languages.

UNIT -IV:

RTOS Based Embedded System Design:

Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling.

UNIT -V:

Task Communication: Shared Memory, Message Passing, Remote Procedure Call and Sockets, Task Synchronization: Task Communication/Synchronization Issues, Task Synchronization Techniques, Device Drivers, How to Choose an RTOS.

TEXT BOOKS:

1. Introduction to Embedded Systems - Shibu K.V, Mc Graw Hill.

REFERENCE BOOKS:

1. Embedded Systems - Raj Kamal, TMH.
2. Embedded System Design - Frank Vahid, Tony Givargis, John Wiley.
3. Embedded Systems – Lyla, Pearson, 2013
4. An Embedded Software Primer - David E. Simon, Pearson Education.

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M. Tech – I Year – I Sem. (VLSI/VLSI Design/VLSI System Design)

DEVICE MODELLING

(Core Elective –II)

UNIT -I:

Introduction to Semiconductor Physics:

Review of Quantum Mechanics, Boltzman transport equation, Continuity equation, Poisson equation.

Integrated Passive Devices:

Types and Structures of resistors and capacitors in monolithic technology, Dependence of model parameters on structures

UNIT -II:

Integrated Diodes:

Junction and Schottky diodes in monolithic technologies – Static and Dynamic behavior – Small and large signal models – SPICE models

Integrated Bipolar Transistor:

Types and structures in monolithic technologies – Basic model (Eber-Moll) – Gunmel - Poon model-dynamic model, Parasitic effects – SPICE model –Parameter extraction

UNIT -III:

Integrated MOS Transistor:

NMOS and PMOS transistor – Threshold voltage – Threshold voltage equations – MOS device equations – Basic DC equations second order effects – MOS models – small signal AC characteristics – MOS FET SPICE model level 1, 2, 3 and 4

UNIT -IV:

VLSI Fabrication Techniques: An overview of wafer fabrication, Wafer Processing – Oxidation – Patterning – Diffusion – Ion Implantation – Deposition – Silicon gate nMOS process – CMOS processes – n-well- p-well- twin tub- Silicon on insulator – CMOS process enhancements – Interconnects circuit elements

UNIT -V:

Modeling of Hetero Junction Devices: Band gap Engineering, Band gap Offset at abrupt Hetero Junction, Modified current continuity equations, Hetero Junction bipolar transistors (HBTs), SiGe

TEXT BOOKS:

1. Introduction to Semiconductor Materials and Devices – Tyagi M. S, 2008, John Wiley Student Edition.
2. Solid State Circuits – Ben G. Streetman, Prentice Hall, 1997

REFERENCE BOOKS:

1. Physics of Semiconductor Devices – Sze S. M, 2nd Edition, Mcgraw Hill, New York, 1981.
2. Introduction to Device Modeling and Circuit Simulation – Tor A. Fijedly, Wiley-Interscience, 1997.
3. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011

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SOFT COMPUTING TECHNIQUES
(Open Elective - I)

UNIT – I: Fundamentals of Neural Networks & Feed Forward Networks
Basic Concept of Neural Networks, Human Brain, Models of an Artificial Neuron, Learning Methods, Neural Networks Architectures, Signal Layer Feed Forward Neural Network :The Perceptron Model, Multilayer Feed Forward Neural Network :Architecture of a Back Propagation Network(BPN), The Solution, Backpropagation Learning, Selection of various Parameters in BPN. Application of Back propagation Networks in Pattern Recognition & Image Processing.

UNIT – II: Associative Memories & ART Neural Networks
Basic concepts of Linear Associator, Basic concepts of Dynamical systems, Mathematical Foundation of Discrete-Time Hop field Networks(HPF), Mathematical Foundation of Gradient-Type Hopfield Networks, Transient response of Continuous Time Networks, Applications of HPF in Solution of Optimization Problem: Minimization of the Traveling salesman tour length, Summing networks with digital outputs, Solving Simultaneous Linear Equations, Bidirectional Associative Memory Networks; Cluster Structure, Vector Quantization, Classical ART Networks, Simplified ART Architecture.

UNIT – III: Fuzzy Logic & Systems
Fuzzy sets, Crisp Relations, Fuzzy Relations, Crisp Logic, Predicate Logic, Fuzzy Logic, Fuzzy Rule based system, Defuzzification Methods, Applications: Greg Viot's Fuzzy Cruise Controller, Air Conditioner Controller.

UNIT – IV: Genetic Algorithms
Basic Concepts of Genetic Algorithms (GA), Biological background, Creation of Offsprings, Working Principle, Encoding, Fitness Function, Reproduction, Inheritance Operators, Cross Over, Inversion and Deletion, Mutation Operator, Bit-wise Operators used in GA, Generational Cycle, Convergence of Genetic Algorithm.

UNIT – V: Hybrid Systems
Types of Hybrid Systems, Neural Networks, Fuzzy Logic, and Genetic Algorithms Hybrid, Genetic Algorithm based BPN: GA Based weight Determination, Fuzzy Back Propagation Networks: LR-type fuzzy numbers, Fuzzy Neuron, Fuzzy BP Architecture, Learning in Fuzzy BPN, Inference by fuzzy BPN.

TEXT BOOKS:

1. Introduction to Artificial Neural Systems - J.M.Zurada, Jaico Publishers
2. Neural Networks, Fuzzy Logic & Genetic Algorithms: Synthesis & Applications -S.Rajasekaran, G.A. Vijayalakshmi Pai, July 2011, PHI, New Delhi.
3. Genetic Algorithms by David E. Gold Berg, Pearson Education India, 2006.
4. Neural Networks & Fuzzy Sytems- Kosko.B., PHI, Delhi,1994.

REFERENCE BOOKS:

1. Artificial Neural Networks - Dr. B. Yagananarayana, 1999, PHI, New Delhi.
2. An introduction to Genetic Algorithms - Mitchell Melanie, MIT Press, 1998
3. Fuzzy Sets, Uncertainty and Information- Klir G.J. & Folger. T. A., PHI, Delhi, 1993.

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M. Tech – I Year – I Sem. (VLSI/VLSI Design/VLSI System Design)

IMAGE AND VIDEO PROCESSING
(OPEN ELECTIVE-I)

UNIT –I:
Fundamentals of Image Processing and Image Transforms: Basic steps of Image Processing System Sampling and Quantization of an image, Basic relationship between pixels.
Image Segmentation: Segmentation concepts, Point, Line and Edge Detection, Thresholding, Region based segmentation.

UNIT –II:
Image Enhancement: Spatial domain methods: Histogram processing, Fundamentals of Spatial filtering, Smoothing spatial filters, Sharpening spatial filters.
Frequency domain methods: Basics of filtering in frequency domain, Image smoothing, Image sharpening, Selective filtering.

UNIT –III:
Image Compression: Image compression fundamentals - Coding Redundancy, Spatial and Temporal redundancy, Compression models: Lossy & Lossless, Huffman coding, Bit plane coding, Transform coding, Predictive coding, Wavelet coding, Lossy Predictive coding, JPEG Standards.

UNIT -IV:
Basic Steps of Video Processing: Analog Video, Digital Video. Time-Varying Image Formation models: Three-Dimensional Motion Models, Geometric Image Formation, Photometric Image Formation, Sampling of Video signals, Filtering operations.

UNIT –V:
2-D Motion Estimation: Optical flow, General Methodologies, Pixel Based Motion Estimation, Block-Matching Algorithm, Mesh based Motion Estimation, Global Motion Estimation, Region based Motion Estimation, Multi resolution motion estimation, Waveform based coding, Block based transform coding, Predictive coding, Application of motion estimation in Video coding.

TEXT BOOKS:
1. Digital Image Processing – Gonzaleze and Woods, 3rd Ed., Pearson.
2. Video Processing and Communication – Yao Wang, Joem Ostermann and Ya–quin Zhang. 1st Ed., PH Int.

REFRENCE BOOKS:
1. Digital Image Processing using MATLAB– Gonzaleze and Woods, 2nd ed., Mc Graw Hill Education, 2010
2. Image Processing Analysis , and Machine Vision- Milan Sonka, Vaclan Hlavac, 3 ed., CENGAGE, 2008
3. Digital Video Processing – A Murat Tekalp, PERSON, 2010
4. Digital Image Processing – S.Jayaraman, S.Esakkirajan, T.Veera Kumar –TMH, 2009

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M. Tech – I Year – I Sem. (VLSI/VLSI Design/VLSI System Design)

SOFTWARE DEFINED RADIO
(Open Elective-I)

UNIT -I:

Introduction: The Need for Software Radios, What is Software Radio, Characteristics and benefits of software radio- Design Principles of Software Radio, RF Implementation issues- The Purpose of RF Front – End, Dynamic Range- The Principal Challenge of Receiver Design – RF Receiver Front-End Topologies- Enhanced Flexibility of the RF Chain with Software Radios- Importance of the Components to Overall Performance- Transmitter Architectures and Their Issues- Noise and Distortion in the RF Chain, ADC and DAC Distortion.

UNIT -II:

Profile and Radio Resource Management : Communication Profiles- Introduction, Communication Profiles, Terminal Profile, Service Profile , Network Profile, User Profile, Communication Profile Architecture, Profile Data Structure, XML Structure, Distribution of Profile Data, Access to Profile Data, Management of Communication Profiles, Communication Classmarks, Dynamic Classmarks for Reconfigurable Terminals, Compression and Coding, Meta Profile Data

UNIT -III:

Radio Resource Management in Heterogeneous Networks

Introduction, Definition of Radio Resource Management, Radio Resource Units over RRM Phases, RRM Challenges and Approaches, RRM Modelling and Investigation Approaches, Investigations of JRRM in Heterogeneous Networks, Measuring Gain in the Upper Bound Due to JRRM, Circuit-Switched System, Packet-Switched System, Functions and Principles of JRRM, General Architecture of JRRM, Detailed RRM Functions in Sub-Networks and Overall Systems

UNIT -IV:

Reconfiguration of the Network Elements : Introduction, Reconfiguration of Base Stations and Mobile Terminals, Abstract Modelling of Reconfigurable Devices, the Role of Local Intelligence in Reconfiguration, Performance Issues, Classification and Rating of Reconfigurable Hardware, Processing Elements, Connection Elements, Global Interconnect Networks, Hierarchical Interconnect Networks, Installing a New Configuration, Applying Reconfiguration Strategies, Reconfiguration Based on Comparison, Resource Recycling, Flexible Workload Management at the Physical Layer, Optimised Reconfiguration, Optimisation Parameters and Algorithms, Optimization Algorithms, Specific Reconfiguration Requirements, Reconfiguring Base Stations, Reconfiguring Mobile Terminals

UNIT -V:

Object – Oriented Representation of Radios and Network Resources:

Networks- Object Oriented Programming- Object Brokers- Mobile Application Environments- Joint Tactical Radio System.

Case Studies in Software Radio Design: Introduction and Historical Perspective, SPEAK easy-JTRS, Wireless Information Transfer System, SDR-3000 Digital Transceiver Subsystem, Spectrum Ware, CHARIOT.

TEXT BOOKS:

1. Software Defined Radio Architecture System and Functions- Markus Dillinger, Kambiz Madani, WILEY 2003
2. Software Defined Radio: Enabling Technologies- Walter Tuttle Bee, 2002, Wiley Publications.

REFERENCE BOOKS:

1. Software Radio: A Modern Approach to Radio Engineering - Jeffrey H. Reed, 2002, PEA Publication.
2. Software Defined Radio for 3G - Paul Burns, 2002, Artech House.
3. Software Defined Radio: Architectures, Systems and Functions - Markus Dillinger, Kambiz Madani, Nancy Alonistioti, 2003, Wiley.
4. Software Radio Architecture: Object Oriented Approaches to wireless System Enginering – Joseph Mitola, III, 2000, John Wiley & Sons.

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M. Tech – I Year – I Sem. (VLSI/VLSI Design/VLSI System Design)

VLSI LABORATORY – I

Note:

- Minimum of 10 programs from Part –I and 2 programs from Part -II are to be conducted.

Design and implementation of the following CMOS digital/analog circuits using **Cadence / Mentor Graphics / Synopsys / Equivalent** CAD tools. The design shall include Gate-level design, Transistor-level design, Hierarchical design, Verilog HDL/VHDL design, Logic synthesis, Simulation and verification.

Part –I: VLSI Front End Design programs:

Programming can be done using any complier. Down load the programs on FPGA/CPLD boards and performance testing may be done using pattern generator (32 channels) and logic analyzer apart from verification by simulation with any of the front end tools.

1. HDL code to realize all the logic gates
2. Design and Simulation of adder, Serial Binary Adder, Multi Precession Adder, Carry Look Ahead Adder.
3. Design of 2-to-4 decoder
4. Design of 8-to-3 encoder (without and with parity)
5. Design of 8-to-1 multiplexer
6. Design of 4 bit binary to gray converter
7. Design of Multiplexer/ Demultiplexer, comparator
8. Design of Full adder using 3 modeling styles
9. Design of flip flops: SR, D, JK, T
10. Design of 4-bit binary, BCD counters (synchronous/ asynchronous reset) or any sequence counter
11. Design of a N- bit Register of Serial- in Serial –out, Serial in parallel out, Parallel in Serial out and Parallel in Parallel Out.
12. Design of Sequence Detector (Finite State Machine- Mealy and Moore Machines).
13. Design of 4- Bit Multiplier, Divider.
14. Design of ALU to Perform – ADD, SUB, AND-OR, 1's and 2's Compliment, Multiplication, and Division.
15. Design of Finite State Machine.
16. Implementing the above designs on Xilinx/Altera/Cypress/equivalent based FPGA/CPLD kits .

Part –II: VLSI Back End Design programs:

Design and implementation of the following CMOS digital/analog circuits using **Cadence / Mentor Graphics / Synopsys / Equivalent** CAD tools. The design shall include Gate-level design/Transistor-level design/Hierarchical design/Verilog HDL or VHDL design, Logic synthesis, Simulation and verification, Scaling of CMOS Inverter for different technologies, study of secondary effects (temperature, power supply and process corners), Circuit optimization with respect to area, performance and/or power, Layout, Extraction of parasitics and back annotation, modifications in circuit parameters and layout consumption, DC/transient analysis, Verification of layouts (DRC, LVS).

1. Introduction to layout design rules
2. Layout, physical verification, placement & route for complex design, static timing analysis, IR drop analysis and crosstalk analysis of the following:
    - Basic logic gates
    - CMOS inverter
    - CMOS NOR/ NAND gates
    - CMOS XOR and MUX gates
    - CMOS 1-bit full adder
    - Static / Dynamic logic circuit (register cell)
    - Latch
    - Pass transistor

Layout of any combinational circuit (complex CMOS logic gate)- Learning about data paths