7. SUBJECT DETAILS

7.4 DIGITAL LOGIC DESIGN

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7.4.7 Experts' Details

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7.4.10 Session Plan

i.Theory

ii. Tutorial plan

7.4.11 Student Seminar Topics

7.4.12 Question Bank

7.4.13 Assignment Questions

7.4.1 OBJECTIVE AND RELEVANCE

In today's world the term digital has become part of our everyday vocabulary because of the dramatic way that digital circuits and digital techniques have become so widely used in almost all areas of life: Computers, Automation, Robots, Medical Science and Technology, Transportation, Entertainment, Exploration and so on. In this subject we will discover the fundamental principles, concepts and operations that are common to all digital systems from the simplest on/off switch to the most complex computer. Digital technology will continue its high speed incursion into current areas of our lifes as well as break new ground in ways we may not even have thought about.
The main Objectives of this course is:

- To understand basic number systems codes and logical gates.
- To understand the Boolean algebra and minimization logic.
- To understand the design of combinational sequential circuits.
- To understand the basic s of various memory.

7.4.2 SCOPE

All of us are familiar with the impact of modern digital computers, communication systems, calculators, watches, mobiles etc. on society. One of the main cost of this revolution is the advent of integrated circuits, which became possible because of the tremendous progress in semiconductor technology in recent years. The operation of these systems and many other systems, is based on the principles of digital techniques and these systems are referred to as digital systems.

Most modern digital circuitry is contained in a programmer device, gate array or full custom integrated circuits. Still, in order to learn how to create those system in a chip we must first understand the building blocks, such as decoders, multiplexers, adders, buffers, latches, registers, counters and so on.

Outcomes of the course:

After this course student could able to design, understand the number systems, combinational sequential circuits. And they should be in a position to continue with computer organization.

7.4.3 PREREQUISITES

An idea on Basic Electronic devices and Boolean Algebra is sufficient.

7.4.4.1 SYLLABUS JNTU

UNIT I

OBJECTIVE

Study of basic philosophy of number systems (Decimal, Binary, Octal, and Hexadecimal).Basic operations like addition and subtraction in these number systems. Characteristics of the binary number system and codes. Methods of converting a binary number to other number systems and vice-versa. To study various Binary codes in use as elementary coding techniques.

students learn to write the Boolean expression for the logic gates . Use Boolean algebra to simplify the complex logic circuits. Use Demorgans theorem to simplify the logic expressions. Construct the truth table for the AND, NAND, OR, NOR, Ex-OR, Ex-Nor and NOT circuits.

SYLLABUS

Digital Systems: Binary Numbers, Octal, Hexadecimal and other base numbers, Number base conversions, complements, signed binary numbers, Floating point number representation, binary codes, error detecting and correcting codes, digital logic gates(AND, NAND,OR,NOR, Ex-OR, Ex-NOR), Boolean algebra , basic theorems and properties, Boolean functions, canonical and standard forms.

UNIT – II

OBJECTIVE

To use Karnaugh maps as tool to simplify and design logic circuits. Conversion of logic expression into a SOP and POS forms. To learn the implementation of Two-level NAND,NOR and other implementations.

SYLLABUS

Gate –Level Minimization and combination circuits , The K-Maps Methods, Three Variable, Four Variable, Five Variable , sum of products , product of sums Simplification, Don't care conditions , NAND and NOR implementation and other two level implementation.

UNIT III

OBJECTIVE

To understand the Basic philosophy of designing digital circuits like Binary adder and subtractors, BCD Adder, Multipliers, Comparators, Encoder, Decoder and Demultiplexer circuits. Designing of MSI circuits like parity bit generators and code converters etc.

SYLLABUS

Combinational Circuits (CC): Design Procedure, Combinational circuit for different code converters and other problems, Binary Adder, subtractor, Multiplier, Magnitude Comparator, Decoders, Encoders, Multiplexers, Demultiplexers.

UNIT IV

OBJECTIVE

To understand the difference between combinational and sequential logic circuits. Operation of latches, flip-flops along with their excitation tables and characteristic equations. To learn the steps involved in designing synchronous sequential circuits and to use state transition tables to design different types of counters, shifters and to study their operation. To learn the minimization of state and flow tables.

SYLLABUS

Synchronous Sequential Circuits: Latches, Flip-flops, analysis of clocked sequential circuits, design of counters, Up-down counters, Ripple counters, Registers, Shift registers, Synchronous Counters. Asynchronous Sequential Circuits: Reduction of state and follow tables, Race free Conditions.

UNIT V

OBJECTIVE

To learn the organization and operation of static and dynamic RAMs, ROMs, Sequential memory and Cache Memory. To understand Memory Address decoding and content accessing process in Random access and Sequential access memories.

SYLLABUS

Memory: Random Access memory, types of ROM, Memory decoding, address and data bus, Sequential Memory, Cache Memory, Programmable Logic Arrays, memory Hierarchy in terms of capacity and access time.

7.4.4.2 SYLLABUS GATE

UNIT I
Complements: Binary Arithmetics, Digital Gates, Boolean Postulates and Simplification of Boolean Expressions

UNIT II
Not applicable

UNIT III
Combinational Logic
Combinational Circuits: Arithmetic circuits, code converters, multiplexers and decoders.

UNIT IV
Synchronous Sequential Logic
Sequential circuits: Latches and flip flops, Counters and Shift registers.

UNIT V
Memories
Static and Dynamic RAMs, Types of ROMs, Memory Addressing.

7.4.4.3 SYLLABUS - IES

UNIT I
Boolean Algebra and logic gates
Boolean algebra, simplification of Boolean function

UNIT II
Gate level minimization
Karnaugh map and applications

UNIT III
Combinational logic
Combinational logic circuits, half/full adder, digital comparator, multiplexers, Demultiplexers.

UNIT IV
Synchronous sequential logic
Flip flops, RS, JK, D & T flip flops
Different types of counters and registers

UNIT V
ROM and their application.

7.4.5 SUGGESTED BOOKS

TEXT BOOKS

T1. Digital Desing - Third edition, M. Morris Mano, Pearson Education.

REFERENCE BOOKS

R1. Switching and Finite Automata Theory - Zvi. Kohavi, Tata McGraw Hill.
R2. Switching and Logic Design, C.V.S. Rao, Pearson Education.
R3. Digital Principles and Design - Donald D. Givone, Tata McGraw Hill, Edition.

R4. Fundamentals of Digital Logic and Micro computer design, 5th Edition. M. Rafiquzzaman John Wiley.

7.4.6 WEBSITES

1. manajntu.com/switching theory logic design notes.
2. www.asic-world.com/digital/tutorial.html
3. www.nptl.com
4. www.adrivingneed.com/digital-stream-electronics
5. http://zebu.uoregon.edu/royfrey/432/digitalnotes.pdf
6. www.educypedia.be/electronics/digitallogic.htm
7. www.en.wikipedia.org/wiki/Digital_circuit
8. www.play-hookey.com/digital/

7.4.7 EXPERTS' DETAILS

INTERNATIONAL

1. Prof. ZVI Kohavi, Ph.D.
   Department of Electrical Engineering and Computer Science,
   TECHNION, Israel Institute of Technology
   Email: www.cs.technion.ac.il/people/kohavi.

2. Stephen Brown, Ph.D.
   Associate Prof. in the department of Electrical and Computer Engineering.
   University of Toronto.
   Email: www.mhhe.com/brownvranesic

NATIONAL

1. Dr. R.P. Jain, Ph.D.
   Principal
   CR State College of Engineering
   Murthal (Sonepat)
   Haryana.
   Email: wwww.mdurohtak.com/mdu/userspace

2. Dr. Ajit Pal, Ph.D.
   Professor,
   Dept. of Computer Science and Engineer
   Indian Institute of Technology,
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   Email: apal@cse.iitgp.ernet.in
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REGIONAL

1. Dr.P.Chandra Sekhar
   Associate Professor,
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2. Prof. Ch.D.V.Paradesi Rao

Professor, ECE
keshav memorial institute of technology.
Hyderabad, A.P. India.
raocdvp@yahoo.co.in

7.4.8 JOURNALS

INTERNATIONAL

1. IEEE, Transaction of circuits and systems
2. journal of Education IETE
3. IEEE, Transactions of VLSI
4. Inventi impact VLSI
5. Journal of Electronic Design Technology

7.4.9 FINDINGS AND DEVELOPMENTS

1. Design and FPGA implementation of a pseudo random bit generation using chaotic maps

Himan Khanzadi, Mohammad Eshghi and shahram Etemadi Borujeni.,IETE Journal of Research vol.59

no.1 Jan.Feb 2013.

2. On the number of linear feedback shift registers with a special structure separal codes, S.Krishnaswamy and

H.K.Pillai, IEEE Trans.on Information Theory , Vol.58, No.3, March 12

3. Design and Implementation of Audio steganography on FPGA by Akabh Mecwan, vijay savani, viren Gajjar, Journal of Electronic Design Tech, vol. issue 1-3 Complilation 2011

4. Design trade-offs in ultra-low-powerdigital nano scale CMOS, A.Tajalli and Y. Leblebici, IEEE Tran. On

Circuits and Systems-I regular papers, Vol.58, No.9, Sept 11.

5. "Design Methodologies for High Performance Noise - Tolerant X-OR and X-NOR circuits",

S. Goel, M.A. Elgamel, M.A. Bayoumi and Y. Hanafy IEEE Transactions on Circuits and Systems, Vol.53, No.4, April 2006.

6. "Low Power small area Digital I/O Cell". Chua-Chin Wang and Yih-Long Tseng - Shian Chen and Ron Hu. IEEE Transactions on Circuits and Systems-II, Vol.52, No.8, Aug 2005.

7.4.10 Session Plan

i.Theory:

S. No.	Topics in JNTU syllabus (for each unit)	Modules and Sub modules made for session plan for each topic	Lecture no.	Suggested Books	Remarks
UNIT-1 : Digital Systems					
1	Introduction to Digital System Design	• Objective • Relevance • Prerequisite and Background • Suggested Books	L1		
2	Binary Numbers, Number Base Conversions	• Review of Number Systems • Binary Number system: Binary to Decimal Conversion and Decimal to Binary Conversion.	L2	T1-Ch.1 T2-Ch.1 R1-Ch.1	IES
3	Octal Numbers, Number Base Conversions	• Octal Number system • Octal to Binary Conversion and Binary to Octal Conversion • Octal to Decimal Conversion and Decimal to Octal Conversion	L3	T1-Ch.1 T2-Ch.1 R1-Ch.1	IES
4	Other Base numbers	• Other non standard base numbers and its conversions.	L4		
5	Hexadecimal Numbers, Number Base Conversions	• Hexadecimal Number system • Hexadecimal to binary conversion and binary to Hexadecimal • Hexadecimal to Octal and Octal to Hexadecimal conversions • Hexadecimal to decimal and decimal to Hexadecimal conversions	L5	T1-Ch.1 T2-Ch.1 R1-Ch.1	IES
6	Complements	• Binary Arithmetic: Addition and subtraction of Binary numbers using r's complement and (r-1)'s complement	L6	T1-Ch.1 T2-Ch.1 R1-Ch.1	GATE /IES

7	Signed Binary Numbers	• Signed Binary Arithmetic : Addition and subtraction of signed Binary numbers .	L7	T1-Ch.1 T2-Ch.1 R1-Ch.1	
8	Floating point Number Representation	• Floating point Number Representations • IEEE Standard	L8		
9	Binary Codes	• Binary weighted and non-weighted codes • Weighted codes: BCD code, 2421, 642-3 codes • Non-weighted codes: Excess 3 code, Gray code, ASCII code.	L9	T1-Ch.1 T2-Ch.1 R1-Ch.1	GATE /IES
10	Error detecting and correcting codes	• Error detecting and correcting codes • Parity bits • Hamming Codes	L10	T1-Ch.7 R1-Ch.1 R2-Ch.1	
11	Digital Logic Gates	• Definition of Binary Logic, logic gates • Graphic Symbol of Algebraic Functions. • Truth Table of following Gates: AND, OR , NOT, NAND, NOR, EX-OR, EX-NOR • Extension to Multiple Gates	L11	T1-Ch.2 T2-Ch.2 R1-Ch.5	GATE
12	Boolean Algebra, Basic Theorems and properties of Boolean algebra	• Postulates and Theorems of Boolean Algebra. • Associative, Cumulative, Distributive Duality, Demorgan's laws	L12	T1-Ch.2 T2-Ch.2 R1-Ch.3	
13	Boolean functions	• Boolean Functions • Duality and Complement of a Boolean function	L13	T1-Ch.2 T2-Ch2 R1-Ch.3	
	canonical and standard forms	• Minterms and Maxterms, • SOP and POS forms • Conversion between canonical forms	L14	T1-Ch.2 T2-Ch.2 R1-Ch.3	
UNIT-2 : Gate Level Minimization and Combinational Circuits					
14	The K-Map method	• Representation of Minimization of K-map • Two variable K-map • Three variable K-map	L15	T1-Ch.3 T2-Ch.5 R1-Ch.4	

15	Four variable map	• Four variable K-map (with don't care terms),Prime implicants	L16		
16	Five variable map	• Five variable K-map (with don't care terms)	L17		
17	Product of Sums Simplification	• Product of Sums Simplification	L18	T1-Ch.3 T2-Ch.5 R1-Ch.4	
18	Don't care conditions	• Don't care conditions	L19		
19	NAND and NOR implementation	Two level implementations • NAND-NAND logic • NOR-NOR Logic	L20	T1-Ch.3 T2-Ch.7 R1-Ch.4	
	other two level implementations	• AND OR- INVERT implementation • OR-AND-INVERT implementation	L21	T1-Ch.3 T2-Ch.7 R1-Ch.4	
UNIT-3 : Combinational Circuits					
20	Combination Circuits Design Procedure	• Combinational Circuits • Design Procedure of combinational Circuits	L22	T1-Ch.5 T2-Ch.8 R1-Ch.5	
		• Implementation of Boolean Functions using gates	L23	T1-Ch.5 T2-Ch.8 R1-Ch.5	
21	Combinational Circuit s for Different code Converters and other Problems	• Design of Binary to Gray code converter • Design of Gray to Binary code converter • Design of BCD to Excess – 3 code converter	L24	T1-Ch.5 T2-Ch.8 R1-Ch.5	
22	Binary Adder	• Half Adder • Full Adder • Ripple carry Adder • Design and Analysis Decimal Adder(BCD)	L25	T1-Ch.5 T2-Ch.5,Ch.20 R1-Ch.5	
23	Binary Subtractor	• Half Subtractor • Full Subtractor • Binary Subtractor	L26	T1-Ch.5 T2-Ch.5,Ch.20 R1-Ch.5	

24	Binary Multiplier	• Design of Binary Multiplier	L27	T1-Ch.5 T2-Ch 18,Ch.20 R1-Ch.4	
25	Magnitude Comparator	• Design of 1-bit Magnitude Comparator • Design of 4-bit Cascaded Magnitude Comparator	L28	T1-Ch.5 T2-Ch.10 R1-Ch.4	
26	Decoders/ DeMultiplexer,	• Design of Decoders / Demultiplexer • Building larger Decoders using smaller configurations	L29	T1-Ch.5 T2-Ch.8 R1-Ch.5 R2-Ch.4	
27	Encoders	• Design of Encoders • Priority Encoder	L30	T1-Ch.5 T2-Ch.8 R1-Ch.5 R2-Ch.4	
27	Multiplexers	• Design and Analysis of Multiplexers Boolean function implementation using MUX	L31		
		• Design Examples	L32		
UNIT-4 : Synchronous Sequential Logic					
28	Sequential Circuits, Latches, Flip-Flops	Memory Elements and Their Excitation Tables • RS Flip-Flop, D Flip-Flop (Level and Edge Triggered)	L33	T1-Ch.6 T2-Ch.11 R1-Ch.9 R2-Ch.6	
		• T Flip-Flop, JK Flip-Flop	L34		
		• Master Slave JK Flip-Flop	L35		
29	Analysis of Clocked Sequential Circuits	• State Equation • State Table • State Diagram	L36	T1-Ch.6 T2-Ch.12 R1-Ch.9 R2-Ch.6	
		• Sequential Circuits • Serial Binary Adder:State Table, State Diagram, State Assignment • Transition and output tables for serial adder	L37		

		• Synthesis of Synchronous Sequential Circuits (sequence detector): • State Table, State Diagram, State Assignment, Transition and output table • Excitation and output map logic diagram of Sequence detector	L38		
30	Design of counters, Synchronous Counters	• Design of Binary Counter • State Table, State Diagram, State Assignment, Transition table • Excitation and logic diagram using flipflops	L39	T1-Ch.6 T2-Ch.13,Ch.14 R1-Ch.9 R2-Ch.7	
31	Registers, Shift Registers	• Register with parallel load, Serial transfer and universal shift register.	L40	T1-Ch.6 T2-Ch.12 R1-Ch.9 R2-Ch.7	
32	Ripple Counters,	• Design of ripple counters-counters with mod numbers,	L41	T1-Ch.6 T2-Ch.12 R1-Ch.9 R2-Ch.7	
33	Up down binary counter	• Design of Up down binary counter Universal Counter	L42		
34	Other Counters	• Counter with unused states, Ring and Johnson counter	L43	T1-Ch.6 T2-Ch.12 R1-Ch.9 R2-Ch.7	
35	Asynchronous Sequential circuits	• Analysis procedure: • Transition table, state table, flow table • Race condition and stability considerations	L44	T1-Ch.9 T2-Ch.23 R2-Ch.8	
		• SR latch, analysis implementation	L45	T1-Ch.9 T2-Ch.23 R2-Ch.8	
		• Flow table, reduction of primitive flow table, transition table, and logic diagram, assigning outputs to unstable states	L46	T1-Ch.9 T2-Ch.23 R2-Ch.8	
36	Reduction of State and Flow Tables	• Implementation table, merging of flow tables, compatible pairs.	L47	T1-Ch.9 T2-Ch.23 R2-Ch.8	

37	Race Free State Assignment	• Three row and four row flow table • Multiple row method	L48	T1-Ch.9 T2-Ch.23 R2-Ch.8	
38	Hazards	• Hazards in combinational and sequential circuits • Implementation with SR latches	L49	T1-Ch.9 T2-Ch.23 R2-Ch.8	
		• Design Examples	L50	T1-Ch.9 T2-Ch.23 R2-Ch.8	
Unit5 : Memories					
39	Introduction, Random Access Memory	• Random Access Memories • Read and write operation • Types of memories	L51	T1-Ch.7	
40	Types of ROMs	• Read only Memory • PROMs • EPROMs • EEPROMs • Flash Memories • Combinational circuit implementation with ROM	L52		
		• Design Examples	L53		
41	Memory Decoding, Address and Data Bus	• Internal construction • Array of RAM chips • Address decoding • Address and Data bus Multiplexing	L54	T1-Ch.7	
42	Sequential memories	• Sequential Memories • Memory access time calculations	L55	T1-Ch.7 R1-Ch.1 R2-Ch.1	
43	Cache Memory	• Cache Memory concept • Its applications	L56	T1-Ch.7 T2-Ch9	
44	Programmable Logic Array	• Block diagram, program table • Combinational circuit implementation with PLA	L57	T1-Ch.7 T2-Ch.9,19	
45	Programmable Array Logic	• Symbol, program table • Combinational circuit implementation with PAL	L58	T1-Ch.7 T2-Ch.9,19	
		• Design Examples	L59	T1-Ch.7 T2-Ch.9,19	
46	Memory Hierarchy interms of capacity and access time	• Memory Hierarchy interms of capacity and access time	L60		

ii. Tutorial Plan

S.No.	Unit	Title	Salient topics to be discussed
1	II	Digital Systems Binary Numbers	Binary Number system: Binary to Decimal Conversion and Decimal to Binary Conversion
2	I	Complements	Addition of binary numbers, subtraction of binary numbers using r's complement, (r-1)'s complement, 2's complement
3	II	Basic Definition, Axiomatic Defination of Boolean Algebra	Postulates and Theorems of Boolean Algebra.
4	II	Basic Theorems and properties of Boolean algebra	Boolean Functions, Compliment of a function, duality
5	III	The Map method	Representation of Minimization of K-map
6	IV	Combination Circuits Analysis Procedure Design Procedure	Combinational Circuits, Analysis and Design Procedure
7	IV	Decimal Adder, Binary Multiplier	Design and Analysis Decimal Adder
8	IV	Multiplexers	Design and Analysis of Multiplexers and Demultiplexers
9	V	Analysis of Clocked Sequential Circuits	Sequential Circuits
10	V	State Reduction and Assignment, Design Procedure	Binary Counter
11	VI	Ripple Counters, Synchronous Counters	Design of ripple counters-counters with mod numbers
12	VI	Other Counters	Design of asynchronous down counter
13	VII	Error Detection and Correction	Hamming code
14	VIII	Design Procedure	Flow table, reduction of primitive flow table, transition table, and logic diagram, assigning outputs to unstable states
15	VIII	Reduction of State and Flow Tables	Implementation table, merging of flow tables, compatible pairs.

7.4.11 STUDENT SEMINAR TOPICS

1. Number systems
2. Number systems
3. Error detecting and correcting codes
4. Two level implementations of Boolean expressions
5. BCD Adder
6. Universal Register
7. Counters and their Applications.
8. Asynchronous Sequential Circuits
9. Races and Hazards
10. Programmable logic devices

7.4.12 QUESTION BANK

UNIT – I

1. a) Convert the following numbers
   i) $(10101100111.0101)_2 = (\ )_{10}$
   ii) $(153.513)_8 = (\ )_{10}$
   b) Perform the subtraction of the given binary numbers using 2's complement
   i) 110110-100111
   ii) 1011.11-101.001 **(Dec 2013)**

2. a) Determine the value of base x, if $(211)_x=(152)_8$.
   b) Add and multiply the following number without converting to decimal. $(15F)_{16}$ and $(A7)_{16}$
   c) The state of a 12-bit register is 010110010111. What is its content if it represents in three decimal digits in BCD? **(Dec 2012)**

3. i. Perform the subtraction with the following unsigned binary numbers by taking the 2's complement of the subtrahend:
   a. 100 – 110000
   b. 11010 – 1101
   ii. Construct a table for 4 -3 -2 -1 weighted code and write 9154 using this code.
   iii. Perform arithmetic operation indicated below. Follow signed bit notation.
   a. 001110 + 110010
   b.101011 – 100110
   iv. Explain the importance of gray code. **(Dec 2011,Nov, June 10)**

4. a) Explain any five properties of the Boolean algebra with example.
   b) Explain with means of truth tables the validation of Demorgan's theorem for three variables (xyz)' = x'+y'+z'. **(Dec 11)**

5. i. Verify that NAND and NOR operations are Commutative but not Associative.
   ii. A certain 4 input gate called LEMON gate realizes the switching function LEMON(A,B,C,D) = BC(A+D) Assuming that the input variables are available in both primed and unprimed form:
   a. show a realization of the function with only three LEMON gates and one OR gate.
   b. Can all switching functions be realized with LEMON/OR logic. **(Dec11, Nov 10)**

6. i Convert the following to require form
   a. $(163.789)_{10} = (\quad)_8$
   b. $(101101110001.00101)_2 = (\quad)_8$
   c. $(292)_{16} = (\quad)_2$
   ii. Find the difference of $(3250 – 72546)_{10}$ by using 10's complement.
   iii. What is meant by self complementing codes. **(Dec 11,Nov 09)**

7. i Write the number from 0 to 9 in any three 4 bit self complementing codes.
   ii. What is the grays code equivalent of HEX number 47A, 331H. **(Dec 11, Nov 09)**

8. i. Reduce the following Boolean expressions.
   a) ((AB)' + A' + AB)'
   b) AB + (AC)' + AB' + C(AB + C)
   c) ((AB' + ABC)' + A(B + AB'))'
   d) AB + A(B+C) + B(B + C).
   ii. Obtain the Dual of the following Boolean expressions.

a) x'y' + xy + x'y
b) xy' + y'z' + x'yz'
c) x' + xy + xz' + xy'z'
d) (x + y)(x + y'). **(Dec 2011,May 2009)**

9. Convert the following numbers.
   i. 10101100111.0101 to Base 10
   ii. $(153.513)_{10} = (\ )_8$
   iii. Find $(3250 - 72532)_{10}$ using 10's complement
   iv. Divide 01100100 by 00011001
   v. Given that $(292)_{10} = (1204)_b$ determine 'b'. **(Nov, June 10)**

10. i. What is the gray code equivalent of the Hex Number 3A7?
    ii. Find the biquinary number code for the decimal numbers from 0 to 9.
    iii. Find 9's complement of $(25.639)_{10}$.
    iv. Find (72532 – 03250) using 9's complement. **(Nov, June 10)**

11. i. Find the possible terms which could be added to the expression using the consensus theorem. Then reduce to a minimum SOP
    A'C'D' + BCD + AB'C' + A'BC
    ii. In a board of directors meeting 4 resolutions A, B, C, D are up to a vote. The vote must be governed by the following rules:
    a. Those who vote for resolution B must also vote for resolution C.
    b. It is possible to vote for both resolutions A & C only if a vote for either B or D is also cast.
    c. Those who vote for either resolution C or D or vote against resolution A must vote for resolution B.

    Each member of the board has 4 switches A, B, C, D which he presses or releases. Depending on whether he is in favor of or against the resolution under the consideration. The switches of each member are the inputs to a circuit associated with that member. Design such a circuit with as few gates as possible. **(Jun 2010)**

12. i. Perform the following using BCD arithmetic.
    a. $1263_{10} - 9687_{10}$
    b. $7672_{10} - 3378_{10}$
    ii. Convert the following:
    a. $997_{10} = (\quad)_{16}$
    b. $257_{10} = (\quad)_8$
    c. $654_{10} = (\quad)_2$
    d. $101_{16} = (\quad)_{10}$ **(June09, May 09)**

13. i. Perform subtraction with the following unsigned decimal numbers by taking 10's Complement of the subtrahend. Verify the result.
    a. 5250 – 1321
    b. 1753 – 8640
    c. 20 – 100
    d. 1200 – 250
    ii. Convert the given gray code number to equivalent binary 1001001011110010 **(June 09,May 09)**

14. i. Explain different methods used to represent negative numbers in binary system.
    ii. Perform the subtraction with the following unsigned binary numbers by taking the 2's complement of the subtrahend.
    a. 11010 – 10110
    b. 11011 – 1001

c. 100 – 110100
d. 1010101 – 1010101
e. 11 – 1101 **(June 09, May 09)**

15. i. State and prove De'Morgans theorems
ii. Prove that NAND and NOR gates are universal gates
iii. Design a 2 input XOR and XNOR using NAND and NOR gates respectively by using only 4 gates each. **(Nov 09)**

16. i. For the given Boolean function F = xy'z + x'y'z + w'xy + wx'y + wxy.
a) Draw the logic diagram
b) Simplify the function to minimal literals using Boolean algebra.
ii. Obtain the Dual of the following Boolean expressions.
a) AB'C + AB'D + A'B'
b) A'B'C + ABC' + A'B'C'D
c) ABCD + ABC'D' + A'B'CD
d) AB + ABC'. **(May 2009)**

17. i. Find the decimal equivalent of the following two's complement numbers.
a. 11111 b. 10001 c. 01010 d. 10011 e. 10101
ii. Explain about error detection and correction with example. **(Nov 08)**

18. i. Perform the following binary multiplication operations
a) 100010 × 001010 = b) 001100 × 011001 = c) 000100 × 010101 =
ii. Write the one's and two's complements of the following example.
a. 0011001 b. 1110011 c. 111111.
iii. Explain, How error occurred in a data transmission can be detected using parity bit. **(Nov 08)**

19. i. Perform the following using BCD arithmetic.
a. 126310 + 968710 b. 767210 + 337810
ii. Convert the following:
a. $99710 = ( )_{16}$ b. $25710 = ( )_{8}$ c. $65410 = ( )_{2}$ d. $10116 = ( )_{10}$ **(Nov 08)**

20. i. Express the following functions in sum of Minterms and product of Maxterms.
a. (xy + z) (y + xz) b. B'D + A'D + BD.
ii. Find the complement of the following and show that F.F' = 0 and F + F' = 1. **(Nov 08)**

UNIT – II

1. Convert the following expression to Sum of Product form
a) (A'+B+C) (A+B'+C') (ABC)
b) (A+B+C') (A'+B'+C') (A'+B+C) **(Dec 2013)**

2. Using Map method simplify the following expression and implement Logic circuit after minimization F(P, Q, R, S) = Σm (0, 1, 4, 8, 9, 10) + d(2, 11). **(Dec 2013)**

3. a) Simplfy the following Boolean expressions using four variable K-map.
wxy+ yz+ xy'z+ x'y.
b) Draw the NAND logic diagram that implements the complement of the following function F(A,B,C,D) =E (0,1,2,3,4,8,9,12) **(Dec 2012)**

4. Obtain a Product of Sums(simplify where possible) A'C'D' +ABD'+ A'CD +B'D. **(Nov 10)**

5. Find all minimal four variable functions which assume the value 1 when the minterms 4, 10, 11,13 are equal to 1 and assume the value 0 when the minterms 1,3,6,7,8,9,12,14 are equal to 1. **(June 10)**

6. i. Construct K-map for the following expression and obtain minimal SOP expression. Implement the function with 2-level NAND - NAND form.

$$f(A,B,C,D) = (A + C + D)(A + B + \overline{D})(A + B + \overline{C})(\overline{A} + B + \overline{D})(\overline{A} + B + \overline{D})$$

ii. Implement the following Boolean function F using the two - level form:
a) NAND-AND
b) AND-NOR $F(A,B,C,D) = \Sigma(0,1,2,3,4,8,9,12)$ **(June 09)**

7. Obtain
i. Sum of product and
ii. Product of sum expressions for the function given below
$F(A,B,C,D) = \Sigma(0,1,2,5,8,9,10)$ **(Nov 08)**

8. Find all the prime implicants for the following Boolean functions and determine which are essential.
$F(A,B,C,D) = \Sigma(0,2,3,5,7,8,10,11,14,15)$. **(Nov 08)**

9. Simplify the following Boolean function using four-variable map.
$F(W,X,Y,Z) = \Sigma(1,3,7,11,15) + d(0,2,5)$. **(Nov 08)**

10. Implement the following Boolean function with NAND gates $F(X,Y,Z) = \Sigma(1,2,3,4,5,7)$. **(Nov 08)**

11. i. If F1 = = Π (3,4,7,8,11,14,15) and $F2 = \Sigma(1,2,4,5,7,8,10,11,12,15)$ obtain minimal SOP expression for $\overline{F_1 \cdot F_2}$ and draw the circuit using NAND gates.
ii. Draw the two -level NAND circuit for the following Boolean - expression: also obtain minimal SOP expression and draw the circuit using NAND gates. **(Nov 08)**

$$(A\overline{B} + C\overline{D})E + BC(A + B)$$

12. i. If F1(A,B,C) = A xor B xor C and F2(A,B,C) = A xnor B xnor C Show that = F1 = F2
ii. Show that A xor B xor AB = A + B
iii. Obtain minimal SOP expression for the complement of the given expression:
And draw the circuit using NOR - gates. $F(A,B,C) = \Pi(1,2,5,7)$. **(Nov 08)**

13. Implement the following Boolean function F using the two - level form:
a. NAND-AND b. AND-NOR $F(A,B,C,D) = \Pi(0, 1, 2, 3, 4, 8, 9, 12)$. **(Nov 08)**

14. i. Obtain minimal SOP expression for the given Boolean expression and hence draw the circuit using NOR gates. F (A,B,C,D) = BC + ABD + A BD + ABCD **(Feb 08)**
ii. Draw NOR-logic diagram that implements the following function: $f(A,B,C,D) = \Sigma(0, 1, 2, 3, 4, 8, 9, 12)$

15. i. Draw the multiple level NOR circuit for the following expression: A(B + C + D) + BCD
ii. Simplify the following functions and implement two level NOR gates:
a. $f(A,B,C,D) = \Sigma(0, 2, 4, 6, 8, 9, 10, 11, 12)$ b. $F(w, x, y, z) = \Pi(5, 6, 9, 11)$ **(Feb 08)**

16. i. Obtain minimal SOP expression for the given Boolean function, using K-map: **(Feb 08, Nov 06,Feb 06)**

F (A,B,C,D) =Σ (0, 1, 4, 6, 8, 9, 10, 12) + d(3, 7, 11, 13, 14, 15)And draw the circuit using 2-input NAND gates.

ii. Obtain minimal POS expression for the Boolean function:

f (A,B,C,D) = Π (0, 1, 2, 3, 4, 6, 9, 10)+d(7, 11, 13, 15) And draw the circuit using 2-input NAND gates.

(Feb 08)

UNIT – III

1. a) Explain the working of 2-bit magnitude comparator.
   b) Draw the logic diagram of 4×1 multiplexer and explain its working. **(Dec 2013)**

2. a) A majority circuit is generated in combinational circuit when the output is equal to 1 if the input variables have more 1's than 0's. The output is 0 otherwise, design a 3-input majority function.
   b) Explain design procedure for a combinational circuit. **(Dec 2012)**

3. i. Design a circuit with four inputs and one output where the output is 1 if the input is divisible by 3 or 7
   ii. A safe has 5 locks: v, w, x, y and z. all of which must be unlocked for the safe to open. The keys to the locks are distributed among five executives in the following manner:
   Mr. A has keys for locks v & x
   Mr. B has keys for locks v & y
   Mr. C has keys for locks w & y
   Mr. D has keys for locks x & z
   Mr. E has keys for locks v & z.
   a. Determine the minimal number of executives required to open the safe.
   b. Find all the combinations of executives that can open the safe. Write an expression f(A,B,C,D,E) which specifies when the safe can be opened as a function of which executives are required.
   c. Who is the essential 'executive' without whom the safe cannot be opened?

   (Nov, Jun 2010)

4. i. Design a BCD to Excess-3 code converter using minimum number of NAND gates.
   ii. Design a BCD to Gray Code converter using 8:1 multiplexers.

   (Dec 11, Nov, Jun10, Nov 08)

5. A Communication system is designed to transmit just two code words A(x_1,x_2,x_3,x_4) = 0010 and B(x_1,x_2,x_3,x_4)=1101.However, due to noise in the system, the received word can have as many as two errors. Design a combinational circuit such that output f1 will be equal to 1 if the received word is A; output f2 will be equal to 1 if the received word is B and output f3 will be equal to 1 if the word received none of these two. **(Nov 10)**

6. i. A combinational circuit has 4 inputs(A,B,C,D) and three outputs(X,Y,Z) XYZ represents a binary number whose value equals the number of 1's at the input:
   a. Find the minterm expansion for the X,Y,Z
   b. Find the maxterm expansion for the X,Y and Z.
   ii. A combinational circuit has four inputs (A,B,C,D), which represent a binary-coded-decimal digit. The circuit has two groups of four outputs - S,T,U,V(MSB digit) and W,X,Y,Z.(LSB digit)Each group represents a BCD digit. The output digits represent a decimal number which is five times the input number. Write down the minimum expression for all the outputs. **(Nov 10)**

7. i. Design a circuit with three inputs(A,B,C) and two outputs(X,Y) where the outputs are the binary count of the number of "ON" (HIGH) inputs.
   ii. Implement 8421 BCD 9's complement subtraction using full adders and other gates.

   (Nov, Jun10)

8. i. Implement Half adder using 4 NAND gates.
   ii. Implement full subtractor using NAND gates only. **(Nov,June 10)**

9. i. Draw the circuit of a Full-Adder using two Half-adders and an OR gate.
   ii. Design a 2-bit comparator using gates. **(Jun 10)**

10. i. Draw the circuit diagram Adder - subtractor circuit for 4 bits and explain its operation.
    ii. Realize Excess - 3 code for the given BCD code using Full adders
    (Use only block diagram of Full adders) **(June 10, May 09)**

11. i. Design a BCD to Gray code converter using 8:1 MUXS.
    ii. Desing a 4 bit carry look ahead adder circuit. **(Nov 09)**

12. i. Design a 4 bit BCD adder using Full adder circuits
    ii. Design a Priority encoder of 4 bit. **(Nov 09)**

13. i. using 3 to 8 line de-multiplexers. Construct 5 to 32 line de-multiplexers. Use active - low Enable input. If necessary use additional logic gates.
    ii. Design a combinational logic circuit with three inputs X, Y, Z and three outputs A, B, C when the binary input is 0, 1, 2, or 3 the binary output is one greater than the input. When the binary input is 4, 5, 6 or 7 the binary output is one less than the input . Draw the circuit using one-full adder and an inverter.(Use only block diagram of Full adder). **(May 09)**

14. i. Implement a Boolean function with a Multiplexer.
    ii. Explain about Tri - State gates in digital systems. **(Nov 08)**

15. i. What is meant by encoder?
    ii. Design a 4 - input priority encoder. **(Nov 08)**

16. i. Explain carry propagation in parallel adder with a neat diagram.
    ii. What is a decoder? Construct a 4×16 decoder with two 3×8 decoders. **(Nov 08)**

UNIT – IV

1. a) What is the difference between latch and flip flop? Explain the working of clocked RS flip flop with a diagram.
   b) Explain working of JK Master Slave flip flop. **(Dec 2013)**

2. a) Explain the working of Mod-10 ripple counter.
   b) Explain the working of serial-in parallel-out shift register with a diagram. **(Dec 2013)**

3. a) Write a procedure for analyzing an asynchronous sequential circuit with SR latch.
   b) Write about Hazards in sequential circuits. **(Dec 2013)**

4. a) Explain Mealy and Moore models.
   b) A sequential circuit has two JK Flip-Flips A and B, two input x and y one output z. The flip flops input functions and circuit output function are follows

   J_A=Bx' + B'y' K_A =B'xy'

   J_B=A'xy K_B=A=xy'

   Z=Axy +Bx'y'

   i) Draw the logic diagram of the circuit.

ii) Tabulate the state table.
iii) Derive the next-state equations for A and B **(Dec 2012)**

5. a) Explain the difference between Synchronous and Asynchronous sequential circuits. What is the difference between stable and unstable states?
b) Explain race free state assignment hazards. Give examples. **(Dec 2012, Nov 08)**

6. Explain the differences among a Truth table, a state table, a characteristic table, and an Excitation table. Also explain the difference among a Boolean equation, a state Equation, a characteristic equation, and a Flip-flop input equation. **(Dec 11, Nov, Jun10)**

7. i. Design an asynchronous up/down counter of 4 bit.
ii. Design an asynchronous modulo-6 counter. Use SR flip flop in the design **(Dec 11, Nov 09)**

8. Explain about the following:
i. Hazards in sequential circuits
ii. Four row flow table
iii. Maximal compatibilities.
iv, Closed covering condition. **(Dec 11,Nov, Jun 10)**

9. i. a) Explain the difference between asynchronous and synchronous sequential circuits.
b) Define fundamental-mode operation.
c) Explain the difference between stable and unstable states.
d) What is the difference between an internal state and a total state.
ii. Explain critical and non critical and non critical races with the help of examples.**(Dec 11, June 09, Nov 08)**

10. a) Design a 4 bit binary synchronous counter with D Filp-Flop.
b) How many Flip-Flop will be complemented in 10-bit ripple counter to reach the next count after the following count 1001100111. **(Dec 11, Jun 10)**

11. Starting from state a, and the input sequences 01110010011, determine the output Sequence for
i. The state table below and
ii. Also the reduced state table to the same state table below and show that the same output sequence is obtained for both. **(Nov 10)**

Present state	Next state		output	
	X=0	X=1	X=0	X=1
a	f	g	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

12. i. Define the following
a. Preset b. Clear c. Race condition d. Race around condition
ii. Draw the schematic circuit of T-Flip-flop. Give its truth table. Justify the entries in the truth table? **(Nov 10)**

13. Explain about the following
    i. Merger Diagrams
    ii. Flow and implication tables. **(Nov 10)**

14. i. Design a 4 bit Ripple counter using T flip flops. Explain using wave forms.
    ii. Compare the merits and demerits of ripple and Synchronous Counters? **(Nov 10,Nov 09)**

15. i. Compare Combinational versus Sequential logic circuits.
    ii. Define the following terms of a flip - flop:
        a) Hold time
        b) Setup time
        c) Propagation delay time. **(June 10, May 09)**

16. Explain about the Following
    i. Serial Transfer in 4-bit shift register
    ii. BCD Ripple Counter
    iii. Universal Shift Register. **(Nov, Jun 10)**

17. i. Draw a diagram showing the Clock Response in Latch and Flip - Flop.
    ii. Draw the characteristics tables for D, T and JK Flip - Flops **(June 10)**

18. i. Draw a neat circuit diagram of positive triggered D flip flop and explain its operation.
    ii. Design a finite state machine which can detect the sequence 0010 by using JK flip flops. **(Nov 09)**

19. i. Draw a neat circuit diagram of a negatives edge triggered JK flip flop and explain its operation.
    ii. What is race around condition? How is it achieved in master slave flip-flops. **(Nov 09)**

20 i. Convert T flip flop to D type flip flop
    ii. Show that the characteristic equation for the compliment output of JK flip flop is $\overline{Q}(T+1)=\overline{J}.\overline{Q}(t)+K.Q(t)$ **(Nov 09)**

21. A sequential circuit with 2 D-flip-flops A and B two inputs (X,Y) and one output 'Z' is specified by the following input equations. $D_A = YX' + XA$, $D_B = BX' + XA$ and $Z = XB$ Obtain logic diagram, state table and state diagram. (**May 09)**

22. Design a sequential circuit with two JK flip - flops A,B with one input X and one out put Y. $A(t + 1) = Ax + Bx$, $B(t +1) = x$ and $Y = Ax' + Bx'$ **(Nov 08)**

23. i. Design a counter with the following repeated binary sequence: 0, 1, 2,3,4,5 using D – flip flops.
    ii. Distinguish between synchronous and asynchronous counters. **(June 09)**

24. Draw the sequential circuit for serial adder using shift registers. full adder and D-FF. Explain its operation with state equations and state table. **(June 09, Nov 08)**

25. i. Design a 4-bit Johnson counter using T - flip flops and draw the circuit diagram and timing diagrams.
    ii. Design a modulo -3 up down synchronous counter using T - flip flops and draw the circuit diagram. **(June 09)**

26. i. Design a 4-bit ring counter using T-flip flops and draw the circuit diagram and timing diagrams.

ii. Draw the block diagram and explain the operation of serial transfer between two shift registers and draw its timing diagram. **(June 09)**

27. A Sequential circuit with two D flip-flops A and B, two inputs x and y and one output z is specified by the following next-state and output equation.
$A(t + 1) = x'y + xA$, $z = B$ and $B(t +1) = x'B + xA$
i. Draw the logic diagram of the circuit.
ii. List the state table for the sequential circuit.
iii. Draw the corresponding state diagram. **(Nov 08)**

UNIT – V

1. a) Explain different types of memory. Explain Error detection and error correction of ROM.
b) Write short notes on programmable array logic. **(Dec 2013, Dec 2012)**

2. Explain about Read only memory in detail? **(Nov 11)**

3. Specify the size of a ROM that will accommodate the truth table for the following Combinational circuit components.
i. A binary multiplier that multiplies two 4-bit numbers.
ii. A 4-bit Adder-subtractor. **(Dec 11, June 10)**

4. Explain about: i. ROM ii. FPGA. **(Dec 11, Nov, June 10)**

5. i. Design a Hamming code encoder to obtain 11 bit code from the circuit use PLAs.
ii. Design a 4 bit number square generated using ROM. **(Dec 11, Nov 09)**

6. i. How many 32K × 8 RAM chips are needed to provide to a memory capacity of 256K Bytes?
ii. How many lines of the address must be used to access 256 bytes? How many of these lines are connected to the address inputs of all chips?
iii. How many lines must be decoded for the chip selected input? Specify the size of the decoder. **(June 10, Nov 08)**

7. i. A 16K * 4 memory uses coincident decoding by splitting the internal decoder into X-selection and Y-selection.
a) What is the size of each decoder and how many AND gates are required for decoding the address?
b) Determine the X and Y selection lines that are enabled when the input address is the binary equivalent of 6000. **(June 09)**

8. List the PAL programming table and draw the PAL structure for the BCD-to-excess-3-code converter. **(June 09)**

9. i. Explain the construction of a basic memory cell and also explain with diagram the construction of a 4*4 RAM
ii. Given a 32*8 ROM chip with an enable input show the external connections necessary to construct a 128 * 8 ROM with four chips and a decoder. **(June 09)**

10. i. Explain the block diagram of a memory unit. Explain the read and write operation a RAM can perform. **(Nov 08)**

11. i. Draw and explain the block diagram of PAL.
    ii. Implement the following Boolean functions using PAL.
    w(A,B,C,D) = ∑m (0,2,6,7,8,9,12,13)
    x (A,B,C,D) = ∑m (0,2,6,7,8,9,12,13,14)
    y (A,B,C,D) = ∑ m (2,3,8,9,10,12,13)
    z (A,B,C,D) = ∑ m (1,3,4,6,9,12,14). **(Nov 08, Feb 06)**

12. Derive the PLA programming table and the PLA structure for the combinational circuit that squares a 3- bit number. Minimize the number of product terms. **(Nov 08, Nov 06)**

13. Design a combinational circuit using a ROM .The circuit accepts a 3bit number & generates an output binary number equal to the square of the input number.

(Nov 08, May 04)

7.4.13 ASSIGNMENT QUESTION

UNIT – I

1. Convert the following to Decimal and then to Octal.
   a) $2A7_{16}$ b) $1BB_{16}$ c) 10110111_2 d) 11011010_2 e)387_{10} f) 677_{10}

2. i. Reduce the following boolean expressions.
      a) AB + A(B + C) + B'(B + D)
      b) A + B + A'B'C
      c) A'B + A'BC' + A'BCD + A'BC'D'E
      d) ABEF + AB(EF)' + (AB)'EF.
   ii. Obtain the Dual of the following Boolean expressions.
      a) x'yz + x'yz' + xy'z
      b) x'yz + xy'z' + xyz'
      c) x'z + x'y + xy'z + yz
      c) x'z + x'y + xy'z + yz
      d) x'y'z' + x'yz' + xy'z'+ xy'z + xyz'.

3. i. Simplify to a sum of 3 terms:
      A'C'D' +AC' +BCD + A'CD' + A'BC + AB'C'
   ii. Given AB' + AB = C, Show that AC' + A'C = B
   iii. Obtain the complement of the following Boolean expressions.
      a) A'B + A'BC' + A'BCD + A'BC'D'E
      b) ABEF + ABE'F' + A'B'EF.

4. i. State and prove De'Morgans theorems
   ii. Prove that NAND and NOR gates are universal gates
   iii. Design a 2 input XOR and XNOR using NAND and NOR gates respectively by using only 4 gates each.

5. i. Add and subtract in binary
      a). 1 1 1 1 and 1 0 1 0 b). 1 1 0 1 1 0 and 1 1 1 0 1
      c). 1 0 0 1 0 0 and 1 0 1 1 0 d). 1 1 0 1 0 0 1 and 1 1 0 1 1
   ii. Explain about error detection and correction codes with example.

UNIT – II

1. i. Construct K-map for the following expression and obtain minimal SOP expression.

Implement the function with 2-level NAND - NAND form.

$$f(A, B, C, D) = (A + C + D)(A + B + \overline{D})(A + B + \overline{C})(\overline{A} + B + \overline{D})(\overline{A} + B + \overline{D})$$

ii. Implement the following Boolean function F using the two - level form:

$F(A,B,C,D) = \Sigma(0,1,2,3,4,8,9,12)$

a) NAND-AND

b) AND-NOR

2. i. Draw the multiple level NOR circuit for the following expression: A(B + C + D) + BCD

ii. Simplify the following functions and implement two level NOR gates:

a) $f(A,B,C,D) = \Sigma(0, 2, 4, 6, 8, 9, 10, 11, 12)$ b) $F(w, x, y, z) = \Pi(5, 6, 9, 11)$

3. i. Find all the prime implicants for the following Boolean functions and determine which are essential.

$F(A,B,C,D) = \Sigma(0,2,3,5,7,8,10,11,14,15)$.

ii. Simplify the following Boolean function using four-variable K-map.

$F(W,X,Y,Z) = \Sigma(1,3,7,11,15) + d(0,2,5)$.

4. i. Convert the following expressions in to sum of products and product of sums.

a) (AB + C) (B + C'D) b) x' + x(x + y')(y + z').

ii. Obtain minimal SOP expression for the complement of the given expression:

And draw the circuit using NOR - gates. $F(A,B,C) = \Pi(1,2,5,7)$.

5. i. Convert the following expression to Sum of Product form

a) (A'+B+C) (A+B'+C') (ABC)

b) (A+B+C') (A'+B'+C') (A'+B+C)

ii. Using Map method simplify the following expression and implement Logic circuit after minimization $F(P, Q, R, S) = \Sigma m(0, 1, 4, 8, 9, 10) + d(2, 11)$.

UNIT – III

1. i. A majority circuit is generated in combinational circuit when the output is equal to 1 if the input variables have more 1's than 0's. The output is 0 otherwise, design a 3-input majority function.

ii. Explain design procedure for a combinational circuit.

2. i. Draw the circuit of a Full-Adder using two Half-adders and an OR gate.

ii. Draw the circuit diagram Adder - subtractor circuit for 4 bits and explain its operation.

3. i. Design a BCD to Excess-3 code converter using minimum number of NAND gates.

ii. Design a BCD to Gray Code converter using 8:1 multiplexers.

4. i. Explain the working of 2-bit magnitude comparator.

ii. Draw the logic diagram of 4×1 multiplexer and explain its working.

5. i. As part of an aircraft's functional monitoring system, a circuit is required to indicate the status of the landing gears prior to landing. Green LED display turns on if all three gears are properly extended when the "gear down" switch has been activated in preparation for landing. Red LED display turns on if any of the gears fail to extend properly prior to landing. When a landing gear is extended, its sensor produces a LOW voltage. When a landing gear is retracted, its sensor produces a HIGH voltage. Implement a circuit to meet this requirement.

ii. In a certain chemical processing plant, a liquid chemical is used in a manufacturing process. The chemical is stored in three different tanks. A level sensor in each tank produces a HIGH voltage when the level of chemical in the tank drops below a specified

point. Design a circuit that monitors the chemical level in each tank and indicates when the level in any two of the tanks drops below the specified point.

UNIT – IV

1. i. Explain about the Derivation of Latch Circuit from Transition Table?
   ii. Explain about the procedure for Analyzing asynchronous sequential circuit with SR Latches

2. Convert the following:
   i. J-K flip-flop to T- flip-flop
   ii. R-S flip-flop to J-K-flip-flop
   iii. J-K flip-flop to D- flip-flop
   iv. R-S flip-flop to D-flip-flop.

3. i. Define BCD Counter and Draw its State table for BCD Counter?
   ii. Explain about 4-bit binary Ripple Counters?
   iii. Compare the merits and demerits of ripple and Synchronous Counters?

4. i. Construct a JK flip-flop using a D flip-flop, a 2-to-1 multiplexer and inverter.
   ii. Explain the working of Mod-10 ripple counter.
   iii. Explain the working of serial-in parallel-out shift register with a diagram

5. Write brief note on
   i. Static and dynamic hazards.
   ii. Merging of flow tables
   iii. Distinguish between Melay and Moore machines in detail
   iv. Serial Transfer in 4 - bit shift Registers

UNIT –V

1. i. Explain error detection and correction Read –only memory
   ii. Explain PLA and PAL With examples

2. i. How many 32K × 8 RAM chips are needed to provide to a memory capacity of 256K Bytes?
   ii. How many lines of the address must be used to access 256 bytes? How many of these lines are connected to the address inputs of all chips?
   iii. How many lines must be decoded for the chip selected input? Specify the size of the decoder.
3. i. Draw and explain the block diagram of PAL.
   ii. Implement the following Boolean functions using PAL.
   w(A,B,C,D) = $\sum$m (0,2,6,7,8,9,12,13)
   x (A,B,C,D) = $\sum$m (0,2,6,7,8,9,12,13,14)
   y (A,B,C,D) = $\sum$ m (2,3,8,9,10,12,13)
   z (A,B,C,D) = $\sum$ m (1,3,4,6,9,12,14).

4. i. List the PAL programming table and draw the PAL structure for the BCD-to-excess-3-code converter.
   ii. Explain about Read only memory in detail?

5. i. Explain the construction of a basic memory cell and also explain with diagram the construction of a 4*4 RAM
   ii. Given a 32*8 ROM chip with an enable input show the external connections necessary to construct a 128 * 8 ROM with four chips and a decoder.