7. SUBJECT DETAILS

7.5 ELECTRONIC DEVICES AND CIRCUITS

7.5.1 Objectives and Relevance

7.5.2 Scope

7.5.3 Prerequisites

7.5.4 Syllabus

i. JNTU

ii. GATE

iii. IES

7.5.5 Suggested Books

7.5.6 Websites

7.5.7 Experts's Details

7.5.8 Journals

7.5.9 Findings and Developments

7.5.10 Session Plan

7.5.11 Question Bank

i. JNTU

ii. GATE

iii. IES

7.5.1 OBJECTIVES AND RELEVANCE

The primary objective of this subject is to get a clear picture of the internal physical behavior of various electronic devices, to analyze and design Electronic Circuits and subsystems using these devices. By learning this subject, students become familiar with the device parameters, the variation of the parameters within a given type and with a change of temperature. The effect of inevitable internal capacitances in circuits, the effect of input and output resistances and loading on circuit operations will be studied. These considerations are of atmost importance to the students. Since the circuits to be designed must function properly and reliably in the physical world, rather than under hypothetical or ideal circumstances, proper care should be taken in design.

7.5.2 SCOPE

The Electronic Devices and Circuits subject is considered as foundation course for Electronics, Electrical, Computer Science Engineers etc. This course covers a syllabus from solid state physics to design of amplifiers, which make the students to familiarise to construct the basic building blocks required for audio and power amplifier design.

7.5.3 PREREQUISITES

Basic concepts of Solid State Physics is required.

7.5.4.1 SYLLABUS - JNTU

UNIT I
P-N JUNCTION DIODE
OBJECTIVE
Characteristics of Mathematical treatment of Junction diode characteristics, P-N Junction diode, Introduction to special semiconductor diode like Zener diode etc. Introduction to special semiconductor diodes like tunnel diode, SCR, Varactor diode and Semiconductor Photo Diode.

SYLLABUS
P-N JUNCTION DIODE: Qualitative Theory of p-n junction, p-n junction a diode, diode equation, Volt-ampere characteristics, Temperature dependence of VI characteristic, ideal versus practical - Resistance levels (Static and Dynamic), Transition and Diffusion Capacitances, Diode equivalent circuits, Load line analysis, Breakdown mechanisms in semi conductor diodes, Zener diode characteristics.
SPECIAL PURPOSE ELECTRONIC DEVICES: Principle of operation and characteristics of Tunnel diode (with the help of Energy Band Diagram) and Varactor diode, SCR, and Semiconductor Photo Diode.

UNIT II
RECTIFIERS AND FILTERS
OBJECTIVE
Basics of Half wave,Full wave and bridge rectifiers. Rectifiers with filters and the voltage regulation using zener diode.

SYLLABUS
The p-n junction as Rectifier, Half wave rectifier, Full wave rectifier, Bridge rectifier, Harmonic components in a rectifier circuit, Inductor filters, Capacitor filters, L-section filters, -section filters, Comparison of filters, Voltage regulation using Zener diode.

UNIT III
BIPOLAR JUNCTION TRANSISTOR
OBJECTIVE
Fundamentals of BJT, Construction Principles, operation and Characteristic curves in different configurations of transistors .Small signal equavalent circuits of BJT.The unit junction transistor

SYLLABUS
The junction transistor, Transistor current components, Transistor as an Amplifier, Transistor construction, BJT operation, BJT symbol, Common base, Common Emitter and Common collector configurations, Limits of Operation, BJT specifications.BJT Hybrid model, Determination of h-parameters from transistor characteristics. Comparison of CB, CE and CC amplifier configurations.UJT and Characteristics.

UNIT IV
TRANSISTOR BIASING AND STABILISATION
OBJECTIVE
Biasing and stabilization techniques for BJT. Amplifier configurations of BJT using h-parameters..

SYLLABUS
Operation point, the DC and AC load lines, Need for biasing, Fixed bias, Collector feedback bias, Emitter feedback bias, Collector-Emitter feedback bias, Voltage divider bias, Bias stability, Stabilization factors, Stabilization against variation in V_{BE} and , Bias compensation using diodes and transistors, Thermal runaway, Thermal stability.Analysis of a transistor amplifier circuit using h-parameters.

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UNIT V
FIELD EFFECT TRANSISTOR AND FET AMPLIFIERS

OBJECTIVE
Fundamentals of FET, Construction Principles, operation and Characteristic curves of transistors. Small signal equivalent circuits of FET. Amplifier configurations using FET.

SYLLABUS
FIELD EFFECT TRANSISTOR:The junction field effect transistor (Construction, principle of operation, symbol) - Pinch-off voltage - Volt-ampere characteristics, The JFET small signal model, MOSFET (construction, principle of operation, symbol), MOSFET characteristics in enhancement and depletion modes.**FET AMPLIFIERS:**FET common source amplifier, Common drain amplifier, Generalized FET amplifier, Biasing FET, FET as voltage variable resistor, Comparison of BJT and FET.

7.5.4.2 SYLLABUS - JNTU- GATE

UNIT I
Simple diode circuits,Characteristics of Tunnel Diode, Varactor diode, SCR, and semiconductor photo diode.

UNIT II
Rectifiers, Filters, Power supplies

UNIT III
BJTs, Characteristics,Equivalent circuits, large and small signals.

UNIT IV

Biasing and bias stability of transistor, Single-transistor configurations,Amplifiers of BJT, Analysis of amplifier.frequency response of amplifiers.

UNIT V

JFETs and MOSFETs,Equivalent circuits, large and small signals. Amplifiers of FET, Analysis of amplifier; frequency response of amplifiers

7.5.4.3 SYLLABUS - IES

UNIT I

Simple diode circuits,Characteristics of Tunnel Diode, Varactor diode, SCR, and semiconductor photo diode.

UNIT II

Rectifiers, Filters, Power supplies

UNIT III

BJTs, Characteristics,Equivalent circuits, large and small signals.

UNIT IV

Biasing and bias stability of transistor, Single-transistor configurationsAmplifiers of BJT, Analysis of amplifier; frequency response of amplifiers.

UNIT V

JFETs and MOSFETs,Equivalent circuits, large and small signals. Amplifiers of FET, Analysis of amplifier; frequency response of amplifiers.

7.5.5 SUGGESTED BOOKS

TEXTBOOKS

T1. Millman's Electronic Devices and Circuits – J. Millman, C.C.Halkias, and Satyabrata Jit, 2 Ed.,1998, TMH.
T2. Electronic Devices and Circuits – Mohammad Rashid, Cengage Learing, 2013
T3. Electronic Devices and Circuits – David A. Bell, 5 Ed, Oxford

REFERENCES:

R1. Integrated Electronics – J. Millman and Christos C. Halkias, 1991 Ed., 2008, TMH.
R2. Electronic Devices and Circuits – R.L. Boylestad and Louis Nashelsky, 9 Ed., 2006, PEI/PHI.
R3. Electronic Devices and Circuits – B. P. Singh, Rekha Singh, Pearson, 2Ed, 2013.
R4. Electronic Devices and Circuits - K. Lal Kishore, 2 Ed., 2005, BSP.
R5. Electronic Devices and Circuits – Anil K. Maini, Varsha Agarwal, 1 Ed., 2009, Wiley India Pvt. Ltd.
R6. Electronic Devices and Circuits – S.Salivahanan, N.Suresh Kumar, A.Vallavaraj, 2 Ed., 2008, TMH.

7.5.6 WEBSITES

1. www.mit.com
2. www.nptel.iitm.ac.in
3. www.faadooengineers.com

4. www.iete.org
5. www.ieee.org
6. www.pearsonhighered.com
7. en.wikipedia.org/wiki/Electronics

7.5.7 EXPERTS' DETAILS

INTERNATIONAL

1. Prof. Trevor J.Trarnton,
   Director of Center for Solid State Electronics Research,
   Arizona State University, Tempe, USA
   Email: khan.tarik@asu.edu,

2. Dr. Manwong,
   Dept. of EEE,
   The Hong Kong University of Science & Technology,
   Kowloon, Hongkong.
   Email: eemwong@ee.ust.hk

3. Dr. I.Irisawa,
   MIRAI-ASET,
   Kawasaki,
   Japan.
   Email: irisawa@mirai.aist.go.jp

4. Dr. Stephen Pearton
   University of Florida,
   Gainesville, USA,
   Email: spear@mse.ufl.edu

NATIONAL

1 Dr. G.S.N. Raju
   Professor
   Andhra University

2. Prof. K.Venkat Rao,
   Principal, GMR Institute of Engineering and Technology
   Rajam
   Vijayanagaram District, A.P.

3. Dr. P.S. Murthy
   Professor,
   Dept.of ECE,
   Indian Institute of Technology,
   Kanpur.

REGIONAL

1. Dr. K.Lal Kishore,
   Registrar,
   JNTU, Kukatpally,

7.5.8 JOURNALS

INTERNARIONAL

1. International Journal of Electornics - Taylor & Francis Ltd.
2. IEEE,Transactions on Electron Devices.
3. IEEE, Transactions on Circuits and systems.
4. IEEE, Transactions on Power electronics

NATIONAL

1. IETE Journal
2. ISOI Journal
3. Journal on Institution of Engineers
4. IETE Journal of Education
5. IETE Journal of Research

7.5.9 FINDINGS AND DEVELOPMENTS

1. Gate Leakage Mechanisms in AlGaN/GaN and AlInN/GaN HEMTs: Comparison and Modeling. IEEE Transactions on Electronic Devices, Vol.60, No. 10, October 2013.

2. Resistance and Threshold Switching Voltage drift behaviour, IEEE Transactions on Electronic Devices, Vol.58, No. 3, March 2011.

3. Interdigit 4H-Sic vertical schottky diode for Beta voltaic applications, IEEE Transactions on Electronic Devices, Vol.58, No. 3, March 2011.

4. A model -based approach for subthreshold operations, IEEE Transactions on Electronic Devices, Vol.58, No. 3, March 2011.

5. Full replacement Gate process for MOSFETs fabrications, IEEE Transactions on Circuits and Systems, Vol.58, No. 3, March 2011..

6. Effects of Variation in the source Doping concetration, IEEE Transactions on Circuits and Systems, Vol.58, No.3, March 2011.

7. Simulation of devices for each epitasial structure for 50nm - gate - length devices, IEEE Transactions on Circuits and Systems, Vol.58, No.3, March 2011..

8. Thermal stress analysis - inside Phase Change Memory (PCM) cell using the measured properties, IEEE Transactions on Circuits and Systems,Vol.58, No.3, March 2011.

9. Subthreshold Electron Mobility in SoI MOSFETs, Tarik Khan, Dragica Vasileska, Member, IEEE and Trevor J. Thornton, Member, IEEE. Prof. Trevor J. Thornton, Dept of EEE. IEEE Transactions on Electron Devices, Vol.52, No.7, July 05.

10. Effects of Substrate Doping on Linearly Extrapolated Threshold voltage of Symmetrical DG MOS Devices, - Xuejie Shi and Dr. ManWong, Dept of EEE. IEEE Transactions on Electron Devices, Vol.52, No.7, July 05.

11. On the origin of Increase in substrate current and Impact Ionization Efficiency in strained-si n-and p-MOSFETs - T. Irisarva, T. Numata, N. Sugiyama and S-I. Takagi. IEEE Transactions on Electron Devices, Vol.52, No.7, July 05.

Session Plan

Sl. No.	Topics in JNTU syllabus	Modules and Sub modules	Lecture	Suggested books	Remarks
		UNIT I			
1		Objective and relevance Prerequisite and background Suggested books	L1		
2	P –N Junction Diode	Review of semiconductor physics Electrons and holes in an intrinsic semiconductor Conductivity of semiconductor	L2	T1-Ch5, R4-Ch2 R2-Ch1	GATE IES
		Carrier concentration in an intrinsic semiconductor Donor and acceptor impurities Charge densities in an semiconductor	L3	T1-Ch5, R4-Ch2 R2-Ch1	GATE IES
3	Qualitative Theory of p-n junction	Qualitative Theory of p-n junction The p-n junction as a diode	L4-L5	T1-Ch5, R2-Ch1 R4-Ch3,	GATE IES
		Band structure of an open circuited pn junction			
4	V-I characteristics of p-n diode	V-I characteristics of p-n diode Diode resistance	L6	T1-Ch5, R2-Ch1	GATE IES
5	Temperature dependence of V-I characteristics	Temperature dependence of V-I characteristics		T1-Ch5, R4-Ch3	GATE IES

6	Transition capacitance	Space charge or transition capacitance Step graded junction and linearly graded	L7-L8	T1-Ch5, R4-Ch3	GATE IES
7	Diffusion capacitance	Diffusion capacitance p-n diode switching times			
8	Breakdown mechanism in semiconductor diode Zener diode characteristics	Breakdown mechanism in semiconductor diode Zener diode characteristics	L9	T1-Ch5, R4-Ch3 R2-Ch1,	GATE IES
9	Principle of operation and characteristics of Tunnel diode (with the help of Energy Band Diagram)	Characteristics of Tunnel Diode	L10	T1-Ch5, R2-16	GATE IES
10	Varactor diode	Characteristics of Varactor diode	L11	T1-Ch5, R2-16	GATE IES
11	SCR	Characteristics of SCR Applications of SCR	L12	T1-Ch5, R2-16	GATE IES
12	Semiconductor Photo Diode.	LED characteristics Photo diode characteristics	L13	T1-Ch19, R2-16	GATE IES
UNIT – II					
9	Half wave rectifier	Half wave rectifier Ripple factor Average voltage, RMS voltage, TUF, Voltage regulation and Rectification efficiency	L14-15	T1-Ch6, R2-Ch2 R4-Ch3	GATE IES

Sl. No.	Topics in JNTU syllabus	Modules and Sub modules	Lecture	Suggested books	Remarks
10	Full wave rectifier	Full wave rectifier Ripple factor Average voltage, RMS voltage,TUF, Voltage regulation and Rectification efficiency	L16-17	T1-Ch6, R2-Ch2 R4-Ch3	GATE IES
11	Bridge rectifier	Ripple factor Average voltage, RMS voltage, TUF, Voltage regulation and Rectification efficiency	L18	T1-Ch6, R2-Ch2 R4-Ch3	GATE IES
12	Harmonic components in rectifier circuits Inductor filter	Harmonic components in rectifier circuits Cancellation of fundamental components and advantage of filtering Inductor filter	L19	T1-Ch6, R4-Ch3	GATE IES
13	Capacitor filter	Capacitor filter Average voltage Ripple factor Problems	L20	T1-Ch6, R4-Ch3	GATE IES
14	L-section filter	L-section filter Average voltage Ripple factor Problems	L21	T1-Ch6, R4-Ch3	GATE IES

15	Π - section filter Multiple Π - section filter	Π- Section filter Multiple Π - section filter	L22	T1-Ch6, R4-Ch3	GATE IES
16	Comparison of various filter circuits in terms of ripple factors	Comparison of various filters	L23	T1-Ch6, R4-Ch3	GATE IES
17	Simple circuit of a regulator using zener diode	Simple circuit of a regulator using zener diode Problems	L24	R2-Ch19, T1-Ch6	GATE IES
	UNIT-III				
18	Junction transistor, Transistor construction, BJT operation, BJT Symbol,	Junction Transistor, Transistor construction, BJT operation, BJT Symbol	L25	T1-Ch7, R2-Ch3	GATE
19	Transistor as a amplifier	The transistor as a amplifier Transistor construction	L26	T1-Ch7, R2-Ch3	GATE
20	Transistor Current components	The detailed study of currents in a transistor	L27	T1-Ch7, R2-Ch3	GATE
21	CB	Characteristics of BJT CB-configuration Input-output characteristics	L28	R4-Ch4, T1-Ch7 R2-Ch3,	GATE IES
22	CE	CE-configuration Input-output characteristics	L29	R4-Ch4, T1-Ch7 R2-Ch3,	GATE IES
Sl. No.	**Topics in JNTU syllabus**	**Modules and Sub modules**	**Lecture**	**Suggested books**	**Remarks**
23	CC	CC-configuration Input-output characteristics	L30	R4-Ch4, T1-Ch7 R2-Ch3	GATE IES

24		Relations between Alpha and Beta, Gamma	L31	T1-Ch7, R2,Ch3	GATE IES
25	Limits of operation and BJT specification	Limits of operation and BJT specification	L32	T1-Ch7, R2,Ch3	GATE IES
26	BJT Hybrid model	Small signal low frequency transistor amplifier circuits Two-port devices and hybrid model	L33	T1-Ch9, R2-Ch5, R4-Ch5	GATE IES
27	Determination of h-parameters from transistor characteristics	Analysis of single stage transistor amplifier using h parameter	L34	T1-Ch9, R2-Ch5, R4-Ch5	GATE IES
28	Comparison of CB, CE and CC amplifier configurations.	Comparison of CB, CE and CC amplifier configurations.	L35	T1-Ch7, R2-Ch8, R4-Ch5	GATE IES
29	The UJT and charactersitics	Construction and Characteristics of Uni junction transistor.	L36	T1-Ch14, R2-Ch21	GATE IES
UNIT-IV					
26	Operating point The DC and AC load lines Need for biasing	Biasing: DC and AC load lines Operating point Criteria for fixing operating point	L37	R2-Ch4, T1-Ch8 R4-Ch6,	GATE IES
27	Fixed bias	Fixed bias circuit Calculation of Q-point Procedure to find Stability factor Problems	L38	R2-Ch4, T1-Ch8 R4-Ch6,	GATE IES

28	Collector feedback bias	Collector to base bias Calculation of Q-point Procedure to find Stability factor Problems	L39	R2-Ch4, T1-Ch8 R4-Ch6,	GATE IES
29	Emitter feedback bias,	Emitter feedback bias circuit Calculation of Q-point Procedure to find Stability factor Problems	L40	R2-Ch4, T1-Ch8 R4-Ch6,	GATE IES
30	Collector-Emitter feedback bias	Collector-Emitter feedback bias circuit Calculation of Q-point Procedure to find Stability factor Problems	L41	R2-Ch4, T1-Ch8, R4-Ch6	GATE IES
31	Voltage divider bias, Bias Stability	Voltage divider bias circuit Calculation of Q-point Procedure to find Stability factor Problems	L42	R2-Ch4, T1-Ch8 R4-Ch6,	GATE IES
32	Stabilization factors Stabilization against variation in V_{BE} and Beta,	Stabilization against variations in V_{BE} and β for self bias circuit Stability factor S^1 and S^{11} Problems Bias compensation	L43	R2-Ch4, T1-Ch8 R4-Ch6,	GATE IES
33	Compensation techniques using diodes and transistors.	Compensation against variation in V_{BE} Compensation against variation in I_{CO}	L44	R2-Ch4, T1-Ch8 R4-Ch6	GATE IES

34	Thermal runway Thermal Stability	Condition to avoid thermal runway	L45	R2-Ch4, T1-Ch8 R4-Ch6	GATE IES
35	Analysis of a transistor amplifier circuit using h-parameters	Measurement of h-parameters for CB, CE, CC (Voltage gain and current gain Input and output impendence) h-parameters Approximate analysis of CB CE and CC amplifier circuits Analysis of various amplifier circuits, Problems	L46 – L47	T1-Ch8, R2-Ch5, R4-Ch5	GATE IES
Sl. No.	**Topics in JNTU syllabus**	**Modules and Sub modules**	**Lecture**	**Suggested books**	**Remarks**
		UNIT V			
36	The junction field effect transistor (Construction principle of operation, symbol)	JFET construction and its static characteristics, pinch-off voltage, CG, CD and CS configurations	L48-49	R4-Ch8, T1, Ch12 R2-Ch5,	GATE IES
37	Pinch-off Voltage - Volt-Ampere characteristics	Pinch-off Voltage,ON resistance r_d(ON), Pinch-off region,the region before Pinch-off, the transfer characteristics.	L50	R4-Ch8, T1, Ch12 R2-Ch6,	GATE IES
38	The JFET small signal model	The JFET small signal model:The Transconductance(g_m),Drain Resistance(r_d)	L51	R4-Ch8, T1-Ch12 R2-Ch6	GATE IES
39	MOSFET (construction principle of operation, symbol),	MOSFET (construction principle of operation, symbol),	L52	R4-Ch8, T1-Ch12 R2-Ch6	GATE IES

40	MOSFET characteristics in enhancement and depletion modes	MOSFET characteristics in enhancement and depletion modes	L53	R4-Ch8, T1-Ch12 R2-Ch6	GATE IES
41	FET common source amplifier	Analysis of a FET Amplifier using small signal model (common source),Voltage gain,Input admittance,Input capacitance, Output Resistance.	L54	T1-Ch12 R2-Ch8	GATE IES
42	Common drain amplifier	Analysis of a FET Amplifier using small signal model (common drain) ,Voltage gain,Input admittance, Output admittance	L55	T1-Ch12 R2-Ch8	GATE IES
43	Generalized FET amplifier	Generalized FET amplifier,Output from the Drain,The CS Amplifier with an unbypassed source resistance,The CG Amplifier ,The output from the source,CD Amplifier.	L56-57	T1-Ch12 R2-Ch8	GATE IES
44	Biasing FET	Biasing FET Fixed Bias, Potential divider,	L58	T1-Ch12 R2-Ch7	GATE IES
45	FET as voltage variable resistor	FET as voltage variable resistor,Applications of VVR.	L59	T1-Ch12	GATE IES
48	Comparison of BJT and FET	Comparison of BJT and FET	L60	T1-Ch12 R2-Ch11	GATE IES

Question Bank

UNIT-I

1. i) Explain the formation of depletion region in an open circuited pn junction with neat sketches.
   ii) The voltage across a silicon diode at room temperature of 300oK is 0.7V when 2mA current flows through it. If the voltage increases to 0.75V, calculate the diode current.

(Nov13)

2. i) Draw the basic structure of Varactor diode and Explain its operation.
   ii) Explain the V-I characteristics of a Tunnel Diode. **(Nov13)**

3. i) Obtain an expression for the current components in a PN junction diode.
   ii) Two identical junction diodes are connected back to back whose VIcharacteristics is Is=0.1uA; Vt=26mv and η=2 are connected .The supply voltageis 15V and the value of the RL=100K.Find the voltage across each diode and current in the circuit. **(Nov13)**
4. In a Zener diode regulator nomial Vi=40V, imax V =45V , imin V =35V, rz=5Ω, 1min I =0mA, 1max I =100mA,, z max I =400mA and z min I =10mA. Find z max P , Ro and Sv.

(Nov13)

5. i. Sketch V-I Characteristics of a PN diode for the following conditions:
   i. R_f =0, Vγ=0, R_r =∞
   ii. R_f =0, Vγ=0.6V, R_r =∞
   iii. R_f =Non-zero fixed value, Vγ=0, R_r =∞
   iv. R_f = Non-zero fixed value, Vγ=0.6V, R_r =∞
   Where Vγ is the cut -in voltage, R_f is the forward dynamic resistance & R_r is the reverse dynamic resistance of the diode.
   ii. Find the voltage drop across each of the silicon diodes shown in Figure .1 at room temperature. Assume that rverse saturation currnt flows in th circuit and the magnitude of the revrsbreakdown voltage is greater than 5V?

(Dec12)

6. i. Draw the structure and two -transistor model of SCR, explain various methods of triggering an SCR.
   ii. With neat sketches, explain the principle of operation of Schottky Barrier Drode.

(Dec12)

7. i. With neat sketches and necessary expressions describe V-I characteristics of a semiconductor photo diode?
   ii. With neat sketches and necessary expressions describe the operation of Varactor diode?

(Nov 11)

8. i. Draw the firing characteristics of SCR and briefly explain it.
   ii. Define the following with respect to SCR
   a. Forward break over voltage
   b. Reverse break over voltage
   c. Holding current
   d. Gate trigger current.

(Nov 11)

9. i. With neat energy band diagrams, explain the V-I characteristics of Tunnel diode. Also discuss the negative resistance property of tunnel diode.
   ii. With neat sketches explain the operation of Schottky Barrier Diode. **(Nov 11)**

10. i. With neat energy band diagrams, explain the V-I characteristics of Tunnel diode. Also discuss the negative resistance property of tunnel diode.
    ii. Draw the two-transistor model of SCR and explain its operation. **(Nov 11)**

11. i. What is Fermi level? By indicating the position of Fermi level in intrinsic, n-type and p- type semicon ductor, explain its significance in semiconductors?
    ii. Sketch V-I characteristics of a PN diode for the following conditions:
    a. Rf = 0, V = 0, Rr = ∞
    b. Rf = 0, V= 0.6V, Rr = ∞
    c. Rf = Non-zero, fixed value, V = 0, Rr = ∞
    d. Rf = Non-zero, fixed value, V = 0. 6V, Rr = ∞
    Where V*f*Á is the cut-in voltage, Rf is the forward dynamic resistance & Rr is the reverse dynamic resistance of the diode. **(Nov 11)**

12. i. What do you understand about the depletion region at a PN junction, with the help of necessary diagrams and derive expression for barrier potential.
    ii. Derive the expression for transition capacitance, CT of a PN diode. **(Nov 11)**

13. i. With the help of necessary sketches explain the potential distribution in an open circuited PN junction.
    ii. With the help of V-I Characteristics, explain the operation of a PN Diode under Forward bias and Reverse bias. **(Nov 11)**

14. i. Explain Avalanche and Zener break down mechanisms in semiconductors and compare them?
    ii. For the Zener diode circuit shown in Figure.1, determine VL, VR , IZ & R **(Nov 11)**

15. i. Derive an expression for total diode current starting from Boltzmann relationship in terms of the applied voltage.
    ii. The reverse saturation current of a silicon p – n junction diode at an operating temperature of 27^0C is 50 nA. Compute the dynamic forward and reverse resistances of the diode for applied voltages of 0.8 V and -0.4 V respectively. **(Nov 10)**

16. i. Explain the operation of silicon p – n junction diode and obtain the forward bias and reverse bias Volt – Ampere characteristics.
    ii. Obtain the transition capacitance C_T of a junction diode at a reverse bias voltage of 12 V if C_T of the diode is given as 15 PF at a reverse bias of 8 V. Differentiate between transition and diffusion capacitances. **(Nov 10)**

17. Difference between
    i. Static and dynamic resistances of a p – n diode.
    ii. Transition and Diffusion capacitances of a p – n diode.
    iii. Volt – Ampere characteristics of a single silicon p – n diode and two identical silicon p- n diodes connected in parallel.
    iv. Avalanche and zener break down mechanisms. **(Nov 10)**

18. i. Define the following terms for a PN diode
    a) Dynamic resistance b) Load line
    c) Difference capacitance d) Reverse saturation current
    ii. A reverse bias voltage of 90V is applied to a Germanium diode through a resistance R. The reverse saturation current of the diode is 50 mA at an operating temperature of 250C. Compute the diode current and voltage for
    a) R = 10 M□ b) R = 100 K□ **(Nov 10)**

19. Describe the following briefly:
    i. Principle of operation of a photodiode.
    ii. Energy band structure and V – I characteristics of a tunnel diode. **(Nov 10)**

20. i. What is schottky effect? Elaborate schottky effect for the functioning of a schottky Barrier diode.
ii. Describe the construction, principle of operation and performance characteristics of a Silicon controlled Rectifier **(Nov 10)**

21. Explain the principle of operation of the following devices:
i. Schottky Barrier diode
ii. Tunnel diode through Energy band diagrams. **(Nov 10)**

22. Explain how a variable capacitance can be built using a varactor diode. **(Nov 10)**

23. i. Explain about diffusion capacitance in detail.
ii. Derive an expression for diffusion capacitance. **(May 09)**

24. i Define Mass Action Law
ii. Explain N type & P type Semiconductors. **(May 09)**

25. i. Explain about semiconductor, Insulator & Conductor with neat sketch.
ii. State the Einstein relationship for semiconductor. State paulis exclusion principle. **(May 08)**

26. i. Explain the volt ampere characteristics of PN diode.
ii. Explain the temperature dependence of VI characteristics. **(May 08)**

27. i. Explain about various current components in a forward biased p-n Junction diode.
ii. Find the value of D.C. resistance and A.C resistance of a Germanium Junction diode at 250 C with Io = 25μA and at an applied voltage of 0.2V across the diode. **(May 07)**

28. i. Explain the formation of depletion region in an open-circuited p-n Junction with neat sketches.
ii. A p-n Junction diode has a reverse saturation current of 30 μA at a temperature of 1250C. At the same temperature find the dynamic resistance for 0.2V bias in forward and reverse direction. **(May 07)**

29. What do you understand by depletion region at p-n Junction? What is the effect of forward and reverse biasing of p-n Junction on the depletion region? Explain with necessary diagrams. **(May 07, 06)**

30. i. Explain the process of break down of a p-n Junction diode due to
a. Avalanche effect
b. Zener effect
ii. Find the concentration of holes and electrons in a p-type silicon at 300^0K assuming resistivity as 0.02-cm. Assume μ_p=475m^2/v-sec, n_i=1.45× 10^{10} per cm^3. **(May 06)**

31. Explain the concept of tunneling with energy band diagrams. **(May 07, 06)**

32. Draw the two transistor version of an SCR and explain its firing characteristics with this circuit. **(May 07, 06)**

33. i. Draw the structure of photo transistor and give its working principle?
ii. What are the advantages of phototransistor over photo diode?
iii. Draw the characteristics of phototransistor. **(Jun 05)**

34. i. Compare the characteristics of a p-n Junction diode, Zener diode and tunnel diode
ii. How do you determine whether a given semiconductor is p-type or n-type? Explain the principle with necessary equations. **(Jun 05, Nov 03)**

35. i. Explain why p-n Junction contact potential cannot be measured by placing a voltmeter across the diode terminal.

ii. With reference to the P-N Junction diode.
a. Distinguish between drift current and diffusion current.
b.Distinguish between diffusion capacitance and transition capacitance **(Jun 05)**

36. i. Explain the term reverse saturation current in the case of a p-n Junction diode
ii. Derive the expression for I_O in a p-n Junction diode. **(Jun 05)**

37. i. Explain about various current components in a forward biased pn Junction diode
ii. Find the value of DC resistance and AC resistance of a germanium Junction diode at 25^o C with I_o = 25 mA and at an applied voltage of 0.2 V across the diode. **(Nov 04)**

38. i. Explain the following terms
a. Storage time
b. Transition time
c. Junction capacitance
ii. Calculate the dynamic forward and reverse resistance of a pn Junction diode when the applied voltage is 0.25 V at T = 300 K given I_o = 2 mA. **(Nov 04)**

39. i. Give the relation between Voltage and Current for a P-N Junction diode
ii. If two similar germanium diodes are connected back to back and the voltage V is imppressed upon, calculate the voltage across each diode and current through each diode. Assume similar value of I_o = 1 □A for both the diodes and □=1
iii. Explain about diffusion capacitance of pn Junction diode. **(Nov 04)**

40. In the case of an open circuited p-n Junction, the acceptor atom concentration is 2.5 x $10^{16}/m^3$ and donar atom concentration is 2.5 x $10^{22}/m^3$. Intrinsic concentration n_i is 2.5 x $10^{19}/m^3$. Determine the value of contact difference of potential. **(Nov 04, Nov 03)**

41. i. Draw the band diagram of pn Junction under open circuit conditions and explain.
ii. Sketch charge density, electric field intensity and potential energy balance for electrons and holes. **(Nov 04)**

42. i. How does the reverse saturation current of diode varies with temperature. Explain
ii. Draw the energy band diagram of p-n diode for no bias, forward bias and reverse bias. **(Jun 04)**

43 i. What are the general specifications of p-n Junction diode
ii. The voltage across a silicon diode at room temperature (300^o k**)** is 0.7 volts when 2 mA current flows through it. If the voltage increases to 0.75 volts, calculate the diode current (V_T=26mV). **(Jun 04)**

44. i. Define law of Junction? Explain about the term cutin voltage associated with p-n Junction diode? How do you obtain cutin voltage from forward V-I characteristics.
ii. Briefly describe about avalanche breakdown and Zener breakdown. **(Jun 04)**

45. i. Explain the term transition capacitance C_T of a pn Junction diode.
ii. Derive the expression for transition capacitance C_T of a diode. **(Nov, May 03)**

46. i. With the help of necessary graphs and sketches explain the potential distribution in an open circuited p-n Junction
ii. Explain about forward bias and reverse bias in the case of a pn Junction diode. **(May 03)**

48. i. Explain about grown and alloy Junctions in the case of a p-n Junction diode.

ii. Determine the forward resistance of a p-n Junction diode, when the forward current is 5 mA at $T = 300^{o}$ K. Assume silicon diode.

(May 03)

49. What are the approximations of forward biased semiconductor diode explain with neat sketches and equivalent circuits .

(May 03)

50. i. Give the two transistor model of a SCR and explain the operation of SCR with the aid of the circuit.

ii. Is SCR current control device or voltage control device - justify you statements. **(Nov 03)**

51. i.Draw the firing characterstics of SCR and briefly explain.

ii. Define the following with respect to SCR.

i. Forward break over voltage

ii. Reverse break over voltage

iii. Holding current

iv. Gate trigger current.

iii. If α_{dc}=0.99 and I_{CBO} = 50 mA, find emitter current. **(Nov 03)**

52. A half wave rectifier circuit employing an SCR is adjusted to have a gate current of 1mA and its forward breakdown voltage is 150V. If a sinusoidal voltage of 400V peak is applied, determine

i. Firing angle

ii. Average output voltage

iii. Average current for a load resistance of 200Ω

iv. Power output. **(Nov 02)**

53. With the help of necessary equations, explain the terms given below:

a. Drift current b.Diffusioncurrent

(Dec 02)

54. Draw the forward and reverse characteristics of a p-n Junction diode and explain them qualitatively? Compare avalanche, Zener and thermal breakdown mechanisms.

(Dec 02)

55. The voltage across a silicon diode at room temperature (300^{o}k**)** is 0.7 volts when 2mA current flows through it. If the voltage increases to 0.75V, calculate the diode current.

(Jun 02)

56. Calculate the threshold voltage at room temperature for diodes rated at 1.0 Amperes. i. Ge: Is=3 micro Amperes ii. Si = 60 nano Amperes **(May 02)**

57. Obtain the static and dynamic resistances of the p-n Junction germanium diode if temperature is 27^{o}C and I_{o}=1μA for an applied bias of 0.2V. Assume K=1.38×10^{-23} J/K.

(Jun 01)

58. A Zener diode and a series resistor are used to get stabilised values of 18 V from a power supply of 22V. If the load resistance is 150 ohms and Iz=12mA. Calculate the value of Rs

(Jun 01)

59. A sample of Si is doped with 10^{17} phosphorus atoms/cm^{3}. Estimate its resistivity. What is the Hall voltage in a specimen 100μm thick if I = 1mA and B=10^{-5}wb/cm^{2}, μ_{n}= 700 cm^{2}/V-s. **(Dec 00)**

60. An n-type germanium sample is 2 mm wide and 0.2 mm thick. A current of 10 mA is passed through the sample (x-direction) and a field of 0.1 weber/m^2 is directed perpendicular to the current flow (z-direction). The developed Hall voltage is -1.0 mV. Calculate the Hall constant and the number of electrons/m^3. **(IES'06)**

61. A silicon abrupt p-n Junction at 300 K has acceptor density, $N_A = 10^{18}$ cm^{-3}, and donor density, $N_D = 10^{15}$ cm^{-3}. If the intrinsic concentration, $N_i = 1.5 \times 10^{10}$ cm^{-3} calculate the built-in voltage, V_1. Derive the relation used. **(IES'05)**

62. Pure silicon has an electrical resistivity of 3000 . If the free carrier density in it is 1.1 x 10^6 m^{-3} and the electron mobility is three times that of hole mobility, calculate the mobility values of electrons and holes. **(IES'04)**

63. Explain the formation of the transition capacitance in a p-n Junction diode. Draw the depletion region in a p-n diode if the p-region is heavily doped. The transition capacitance for such a diode having specific value of N_d is given by $C_T = 1.4 \times 10^8 V_B^{-1/2}$ pf /m^2 Where V_B is the reverse bias voltage. The specific value of N_d is given by $C_T = 1.4 \times 10^8 V_B^{-1/2}$ pf /m^2 Where V_B is the reverse bias voltage. The device is to be used as varactor requiring a capacitance value of 140 pf at 1 volt. Explain how it can be realized. **(IES'03)**

64. An intrinsic silicon, the Fermi level lies near the middle of the bandgap. How does the Fermi level move when it is doped with i. phosphorus, and ii. boron atoms ? Can the Fermi level be pushed up into the conduction band ? if Yes, explain how. It not, explain why. **(IES'01)**

65. Explain why a doped semiconductor that is extrinsic at normal temperatures, behaves as an intrinsic material above a certain temperature. Upon which parameters will this temperature depend?**(IES'01)**

66. "An n-type semiconductor has more number of electrons than holes, hence it has a net negative charge". Justify or nullify the above statement. **(IES'01)**

67. Sketch the terminal current voltage characteristics of the following diodes under both forward and reverse biased conditions. **(IES'01)**
    i. p-n Junction diode.
    ii. Zener diode
    iii. Tunnel diode
    iv. Shockley diode
    v. Light-emitting diode.

68. Find the voltage drop across each of the silicon Junction diodes connected in back to back fashion at room temperature. Assume that reverse saturation current flows in the circuit and the magnitude of the reverse breakdown voltage is greater than 5 volts. **(IES'01)**

69. Show that the semiconductor has minimum conductivity at a given temperature when $N = n_i$ & $P = n_i$. **(IES'98)**

70. When the current through a Zener diode increases from 20 mA to 30 mA the voltage across it changes from 5.6 V to 5.65 V. what is the voltage across the Zener when the current is 35 mA? **(IES'98)**

71. A germanium diode has reverse saturation current of □□ at 125^0 C. What are the dynamic forward and reverse resistances for a bias 0.2 V at this temperature. **(IES'97)**

72. A silicon diode showed currents of 2 m A and 10 mA respectively when the diode voltages were 0.6 V and 0.7V. Estimate the operating temperature of the diode Junction. **(IES'94)**

73. Explain the working of a p-n Junction diode. In an abrupt p-n Junction silicon diode, the conductivities of p-type and n-type silicon are 100 $(\square\text{-cm})^{-1}$ The intrinsic carrier concentration for silicon is $1.5x10^{10}$ cm^{-3} Calculate the value of potential barrier for the unbiased diode at 300^0 K. For silicon, $\square_p$=500cm^2 / V-sec and $\square_n$ = 1300 CM^2 / V-s Iec. **(IES'91)**
(Electric charge e=1.6 $X10^{-19}$ C: Boltzamann's constant k=1.38 $X10^{-23}$ JK^{-1}

74. A sample of germanium shown no Hall effect. If the mobility of electrons in germanium is 3500 cm^2 /V sec and that of the holes is 1400 cm^2 /V sec, what fraction of the current in the sample is carried by electrons? Prove formula used. **(IES'90)**

75. Derive expressions for Fermi level in case of n-type and p-type semiconductors. Draw the band structure of P-N Junction diode and indicate Fermi levels **(AU'Dec 00)**

76. In a *pn* junction diode under reverse bias, the magnitude ofelectric field is maximum at
   i. the edge of the depletion region on the *p*-side
   ii. the edge of the depletion region on the *n*-side
   iii. the *pn* junction
   iv. the centre ofthe depletionregiononthe *n*-side **(GATE '07)**

77. The values of voltage (V_D) across a tunnel-diode corresponding to peak and valley currents are V_P and V_V respectively. The range of tunnel-diode voltage $V_D$for which the slope of its I-$V_D$chracteristics is negative woud be

   i. $V_D < 0$

   ii. $0 < V_D < V_P$

   iii. $V_P < V_D < V_V$

   iv. $V_D > V_V$ **(GATE'07)**

78. The concentration of minority carriers in an extrinsic semiconductor under equilibrium is
   i. directly proportional to the doping concentration
   ii. inversely proportional to the doping concentration
   iii. directly proportional to the intrinsic concentration
   iv. inversely proportional to the intrinsic concentration **(GATE'06)**

79. Under low level injection assumption, the injected minority carrier current for an extrinsic semiconductor is essentially the

i. diffusion current
ii. drift current
iii. recombination current
iv. induced current **(GATE'06)**

80.. Find the correct match between Group1 and Group2:

Group1	Group2
(E) Varactor diode	(1) Voltage reference
(F) PIN diode	(2) High frequency switch
(G) Zener diode	(3) Tuned circuits
(H) Schottky diode	(4) Current controlled attenuator

(A) E-4 F-2 G-1 H-3 (B)E-2 F-4 G-1 H-3
(C)E-3 F-4 G-1 H-2 (D)E-1 F-3 G-2 H-4 **(GATE'06)**

UNIT-II

1. a) Draw the circuit diagram of a Full wave bridge rectifier. Explain the operation of circuit with relevant waveforms.
b) A Full wave single phase rectifier makes use of 2 diodes, the internal forward resistance of each is considered to be constant and equal to 30Ω. The load resistance is 1KΩ. The transformer secondary voltage is 200-0-200V(rms).Calculate
i) DC load current ii) DC output voltage
iii) Peak Inverse Voltage of each diode iv) RMS voltage across each diode. **(Nov 13)**

2. i. In a full- wave rectifier with capacitor filter, show that the rupple voltage is inversly proportional to the capacitance of the capacitop and is proportional to the load cirrent. Calculate the ripple voltagewhen C= 100F and I_{DC} = 10mA.
ii. Draw th circuit of Zener voltag regulator. Explain its operation with neat characteristics and also derive expressions for minimum and maximum values of source resistor for the Zener diode to work as a voltage regulator.
(Dec 12)

3. i. Draw the block diagram of a regulated power supply and explain its operation.
ii. A full wave bridge rectifier having load resistance of 100 is fed with 220V, 50Hz through a step-down transformer of turns ratio 11:1. Assuming the diodes ideal, find
a. DC output voltage
b. Peak inverse voltage
c. Rectifier efficiency. **(Nov 11)**

4 i. With neat sketches explain the operation of a FWR with L- section filter & derive the expression for its ripple factor. Also explain the necessity of a bleeder resistor in a practical L- section filter.
ii. Determine the ripple factor of an L-section filter comprising a 10H choke and 8F capacitor, used with a FWR. The DC voltage at the load is 50V. Assume the line frequency as 50Hz. **(Nov 11)**

5. i. Define the following terms of a rectifier and filter:
a) Ripple Factor b) Regulation
c) Rectification Efficiency d) Form Factor

ii. What is the ripple factor if a power supply of 220 V, 50 Hz is to be Full Wave rectified and filtered with a 220 □F capacitor before delivering to a resistive load of 120 □? Compute the value of the capacitor for the ripple factor to be less than 15%. (Nov 10)

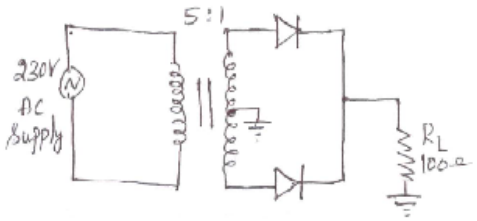
6. i. Derive expressions for ripple factor of a Full Wave Rectifier with and without a capacitive filter.
   ii. Compute the average and RMS load currents, TUF of an unfiltered centre tapped Full Wave Rectifier specified below.
   Input voltage to transformer = 220 V/50 Hz.
   Step down ratio of centre tapped transformer = 4:1(Primary to each section secondary).
   Sum of transformer secondary winding in each secondary segment and diode forward resistance = 100 □.
   Load resistance, R_L = 220 □. **(Nov 10)**

7. i. Define Ripple factor and form factor. Establish a relation between them.
   ii. Explain the necessity of a bleeder resistor in an L – section filter used with a Full Wave filter.
   iii. Compute ripple factor of an L – section choke input filter used at the output of a Full wave rectifier inductor capacitor values of the filter are given as 10 H and 8.2 F respectively. **(Nov 10)**

8. i. List out the merits and demerits of Bridge type Full Wave rectifiers over centre tapped type Full Wave rectifiers.
   ii. The secondary voltages of a centre tapped transformer are given as 60V-0V-60V the total resistance of secondary coil and forward diode resistance of each section of transformer secondary is 62□. Compute the following for a load resistance of 1 K□.
   a) Average load current
   b) Percentage load regulation
   c) Rectification efficiency
   d) Ripple factor for 240 V/50Hz supply to primary of transformer.
   e) What is bleeder resistance in L – section filters? **(Nov 10)**

9. Draw the circuit diagram of a FWR
   i. With centre tap connection and
   ii. Bridge connection and explain its operation **(May 09)**

10. . Determine
   i. DC output voltage.
   ii. PIV
   iii. Rectification effeminacy of the given circuit figure



(**May 09,08)**

11. Derive all the necessary paramters of HWR (May 09)

12. i. Write a short notes on multiple L-section and multiple H-section filter.
   ii. Compare all the filter circuits from the point of view of ripple factor. (May 09)

13. A voltage of 200 cos wt is applied to HWR with load resistance of 5 K. find the maximum d.c current component, r.m.s. current, ripple ractor, TUF and rectifier efficiency. (May 08)

14. Draw the circuit diagram of a FWR:
    i. With centre tap connection and
    ii. Bridge connection and explain its operation. (May 08)

15. i. Draw the circuit diagram of HWR. Explain its working. What is the frequency of ripple in its output
    ii. A HWR circuit supplies 100mA d.c to a 250 load. Find the d.c output voltage, PIV rating of a diode and the r.m.s. voltage for the transformer supplying the rectifier. **(May 08)**

16. i. Define the following terms of a half wave rectifier with resistive load.
    a. Ripple factor.
    b. Peak inverse voltage.
    c. Rectification effciency.
    ii. A 230 V, 60Hz voltage is applied to the primary of a 5:1 step down, center tapped transformer used in a full wave rectifier having a load of 900 .If the diode resistance and the secondary coil resistance together has a resistance of 100 , determine
    a. dc voltage across the load.
    b. dc current flowing through the load.
    c. dc power delivered to the load.
    d. PIV across each diode
    e. Ripple voltage and its frequency. **(May 07)**

17. i. Explain about the regulation characteristics of Zener diode with a circuit and waveforms.
    ii. A full wave rectifier circuit uses two silicon diodes with a forward resistance of 20 each. A d.c. voltmeter connected across the load of 1k reads 55.4 volts. Calculate
    a. RMS current
    b. Average voltage across each diode
    c. ripple factor
    d. Transformer secondary voltage rating. **(May 07)**

18. i. Define the terms as referred to FWR circuit. **(May 07,06)**
    a. PIV b. average d.c. voltage
    c. RMS current d. ripple factor.
    ii. A full wave rectifier (FWR**)** supplies a load requiring 300V at 200mA. Calculate the transformer secondary voltage for
    a. a capacitor inpur filter using a capacitor of 10 µF.
    b. a choke input filter using a choke of 10 H and a capacitance of 10µF. Neglect the resistance of choke.

19. i. Draw the circuit diagram of full-wave rectifier with inductor filter.
    ii. A full-wave rectified voltage of 18V peak is applied across a 500µF filter capacitor. Calculate the ripple and d.c. voltages if the load takes a current of 100mA. **(May 07)**

20. i. Explain why a bridge rectifier is preferred over a centre-tap rectifier.
    ii. Explain the necessity of a bleeder resistor.
    iii. A diode has an internal resistance of 20 ohms and 1000 ohms load from a 110V rms source of supply. Calculate
    a. the effciency of rectification
    b. the percentage regulation from no load to full load. **(May 06)**

21. A full wave rectifier has a center tap transformer of 100-0-100V and each one of the diodes is related at I_{max}=400mA and I_{av}=150 mA. Neglecting the voltage drop across the diodes.
    i. The value of load resistor that gives the largest d.c. power output.
    ii. D.C load voltage

iii. D.C load current
iv. PIV of each diode **(Jun 05)**

22. i. Compare Half wave, Full wave and Bridge rectifier.
ii. What is the necessity of having filter in power supply? Obtain the ripple factor of a full wave rectifier with shunt capacitor filter **(Jun 05)**

23. i. Discuss a full wave rectifier with filter
ii. Compare the performance of inductive, L-section and section filters **(Jun 05)**

24. i. A 15-0-15 volts (rms) ideal transformer is used with a full wave rectifier circuit with diodes having forward drop of 1 volt. the load is a resistance of 100 and a capacitor of 10,000 f is used as a filter across the load resistance calculate the dc load current and voltage.
ii. Draw the circuit diagram of a bridge rectifier circuit with Pi section followed by L-section filter and explain its operation. **(Nov, Jun 05)**

25. i. Derive the expression for ripple factor in a fullwave rectifier using an inductor filter
ii. Compare the performance of series inductor, L section and section filters
iii. In a fullwave rectifier using an LC-filter L = 10H, C = 100 mF and R_L = 500 ohms
Calculate I_{dc}, V_{dc} for an input V_i=30sin(100t). **(Nov 04)**

26. i. Show that for a half-wave rectifier
% where R_f is forward resistance of diode and R_L is the load resistance
ii. Derive the expression for maximum efficiency of a full wave rectifier. **(Nov 04)**

27. i. Show that maximum dc output power $P_{dc} = V_{dc} \times I_{dc}$ in a halfwave single phase circuit occur when the load resistance R_L equals diode resistance R_f
ii. Draw the circuit of a full-wave rectifier using center tapped transformer to obtain an output dc voltage V_{dc} = 18 V at 200 mA. And V_{dc} no load equals to 20V. Assume suitable value of R_f and transformer resistance and also mention transformer rating and sketch the input and output waveforms. **(Nov 04)**

28. i. What is the cause of surge in rectifier circuits using capacitor filter? How is the current limited.
ii. In a full wave rectifier the required dc voltage is 9 volts and diode drop is 0.8V. Calculate AC rms input voltage required in the case of bridge rectifier circuit and center tapped full wave rectifier circuit.
iii. Derive the expression for the ripple factor of HWR and FWR. **(Nov 04)**

29. i. For a FWR with shunt capacitance filter. Derive expression for ripple factor using approximate analysis
ii. Why filter circuit is necessary in rectifiers. Give the list of different filters used in section and their merits and demerits. **(Nov 04)**

30. i. Draw the circuit diagram of a rectifier. Explain the operation of the circuit with relevant waveform.
ii. A bridge rectifier uses 4 identical diodes having forward resistance of 5 ohms each. Transformer secondary resistance is 5 ohms and the secondary voltage is 30 Volts (rms). Determine the DC output voltage for I_{dc} = 20 mA and the value of the output ripple voltage. **(Nov 04)**

31. i. Explain the circuit diagram of a single phase full wave bridge rectifier and sketch the input and output waveforms.
ii. Define percentage of regulation and prove that the regulation of both half-wave and full-wave rectifier is given by percentage regulation is equal to **(Nov 04)**

32. Compare the ripple factors achieved in half wave and full wave rectifier cirucits. **(Dec 04)**

33. i. Explain the following terms
a. ripple factor
b. peak inverse voltage
c. efficiency
d. TUF
e. form factor
f. peak factor

ii. A HWR has a load of 3.5 k ohms. If the diode resistance and the secondary coil resistance together have a resistance of 800 ohms and the input voltage has a signal voltage of 240V, calculate
a. peak, average and rms value of current flowing
b. dc power output
c. ac power input
d. efficiency of the rectifier **(Nov 03)**

34. Define the following terms of a halfwave rectifier with resistive load
a. ripple factor
b. peak inverse voltage
c.rectificationefficiency **(May 03, June 00)**

35. i. What is a rectifier? Show that a p-n diode acts as a rectifier.
ii. Draw the circuit diagram for a half-wave rectifier and explain its operation.
iii. Explain the various types of filter used in power supplies. **(Nov 03)**

36. i. Define the following terms
a. Transformer utilization factor
b. Form factor and ripple factor of a halfwave rectifier with resistive load and derive the expression for the same.

ii. A halfwave rectifier has a load of 3.5 k □. If the diode resistance and secondary coil resistance together have a resistance of a 500 □ and the input voltage has a signal voltage of peak value 240 V, calculate
a. peak, average and rms value of current flowing
b. dc power output
c. ac power input
d. efficiency of the rectifier **(May 03, June 00)**

37. A simple full wave bridge rectifier circuit has an input voltage of 240 V a.c. r.m.s. Assume the diodes to be ideal. Find the output d.c current ,d.c. voltage, r.m.s values of output currents and voltages and the peak inverse voltage that appears across the non-conducting diode. Assume load resistance to be 10 K □ . **(IES'01)**

38. A silicon single phase full wave bridge rectifier circuit is shown. Explain what happens if the transformer and the load positions are interchanged. **(IES'98)**

39. By a drawing a suitable diagram explain the operation of a full-wave centre-tapped rectifier circuit.
A centre-tapped transformer used in a full-wave rectifier circuit has a 250 V primary winding and a 9-0-9 V secondary winding. The load resistance is 150 □. Calculate the d.c output voltage, d.c load current and the peak inverse voltage rating required for the diodes, if they are assumed ideal.
(IES'90)

40. In a full-wave rectifier, the value of load resistance is 5000 □ . Each diode has idealized characteristics having slope corresponding to a resistance 800□. Voltage applied to each diode has amplitude of 300 V and frequency equal to 50 Hz.,
Calculate
i. peak, average and r.m.s. values of current,
ii. d.c. power output and total power input,
iii. rectifier efficiency,
iv. form factor, and

v. ripple factor. **(IES'90)**

41. What are the readings of DC voltmeter,RMS reading voltmeter and true RMS reading voltmeter connected accross the load of a full wave rectifier. **(IES'90)**

42. For the Zener diode shown in the figure, the Zener voltage at knee is 7V, the knee current is negligible and the Zener Dynamic resistance is 10□.if the input voltage(Vi) range isfrom 10 to 16V, the output voltage (Vo) ranges from

i. 7.00 to 7.29V ii. 7.14 to 7.29
iii. 7.14 to 7.43 V iv. 7.29 to 7.43 V **(GATE'07)**

UNIT-III

1. i) What is Early Effect? How does it modify the V-I characteristics of a BJT?
ii) The reverse leakage current of the transistor, when connected in CB configuration is 0.2μA, while it is 18μA when the same transistor is connected in CE configuration. Calculate α and β of the transistor. [9+6] **(Nov 13)**

2. i) Sketch a family of CE input characteristics for a transistor and explain its Operation? **(Nov 13)**

3. i. Explain Early effct and its consequences in a BJT. Also draw the Ebers -Moll model of a PNP transistor.
ii. In the circuit shown in Figure.2, a silicon transistro with = 100, V_{BE} = 0.7V and region or in saturation region? **(Dec 12)**

4. i. With a neat diagram explain the various current components in an NPN bipolar junction transistor & hence derive general equation for collector current, IC?
ii. What is Early-effect; explain why it is called as base-width modulation? Discuss its consequences in transistors in detail? **(Nov 11)**

5. i. Draw the circuit diagram of NPN transistor in Common Emitter(CE) configuration. With neat sketches and necessary equations, describe its static input-output characteristics and clearly indicate the cut-off, saturation & active regions on the output characteristics? **(Nov 11)**
ii. Calculate the values of IC and IE for a transistor with a'dc = 0.99 and ICBO = 5μA, if IB is measured as 20 μA.

6. i. Draw the circuit diagram of NPN transistor in Common Base (CB) configuration. With neat sketches and necessary equations, describe its static input- output characteristics and clearly indicate the cut-off, saturation & active regions on the output characteristics?
ii. With reference to a BJT, define the following terms and explain:
i) Emitter efficiency.
ii) Base transportation factor.
iii) Large signal current gain. **(Nov 11)**

7. i. Draw the circuit diagram of NPN transistor in Common Collector (CC) configuration. With neat sketches and necessary equations, describe its static input- output characteristics and clearly indicate the cut-off, saturation & active regions on the output characteristics?
ii. Derive the relationship among a, b and in transistors? **(Nov 11)**

8. i. Draw the circuit diagram of NPN transistor in Common Emitter(CE) configuration. With neat sketches and necessary equations, describe its static input-output characteristics and clearly indicate the cut-off, saturation & active regions on the output characteristics?

ii. Calculate the values of IC and IE for a transistor with dc = 0.99 and ICBO = 5A, if IB is measured as 20 A. **(Nov 11)**

9. i. With the help of input & output characteristics, explain the operation of a BJT in Common Emitter Configuration.
   ii. For an NPN transistor with aN = 0.98, JCO = 2mA and IEO = 1.6mìA connected in Common Emitter Configuration, calculate the minimum base current for which the transistor enters into saturation region. VCC and load resistance are given as 12 V and 4.0 KW respectively. **(Nov 10)**
10. i. With the help of a hybrid equivalent circuit of a BJT amplifier, derive expressions for voltage gain and current gain when the source and load resistances of finite values are connected.
   ii. List out the typical values of h . parameters in the three BJT configurations (CE, CB and CC).
   iii. Describe how hie and hfe can be determine from BJT characteristics. **(Nov 10)**
11. Define all the four hybrid parameters of a BJT in CE configuration. Draw the circuit and its equivalent circuit. **(Nov 10)**

12. i. Compare the characteristics of a BJT in CB, CE and CC configurations.
   ii. A Silicon BJT is connected in common Emitter configuration with collector – to – Base bias. Calculate the base resistance R_b for the quiescent collector – to – Emitter voltage, V_{CE} has to be 4 V. V_{CC} and R_C are given as 12 V and 1 K□ respectively. Assume □= 100, V_{BE} to be zero volts. Also find the stability factor of the circuit. **(Nov 10)**

13. i. Describe the significance of the terms, '□' and '□'. Establish a relation between them.
   ii. A transistor is operated at a forward emitter current of 2 mA and with the collector open – circuited. Assuming □$_N$ = 0.98, I_{EO} = 1.6 µA and I_{CO} = 2 µA, determine
   a) The junction voltages V_C and V_E
   b) The collector to Emitter voltage V_{CE}
   c) The region of transistor operation (Saturation/Active/Cut-off).
   Assume any other values necessary. **(Nov 10)**

14. i. Describe the functioning of a BJT in common base configuration.
   ii. Determine the collector current of a BJT with both of its junctions reverse biased. Assume I_{CO} = 5µA, I_{EO} = 3.58 µA, α = 0.98 and any other parameter values as required.
   iii. How do you identify the region of operation of a BJT to be saturation region from the values of various circuit currents? **(Nov 10)**

15. With necessary diagram explain the input & output characterisitics of common emitter configuration.(May 09)

16. i. Write short notes on Emitter efficiency.
   ii. Write short notes on Transport factor.
   iii. Large signal current gain. (May 09,08)

17. i. Define a Transistor.
   ii. What are the differences between Bipolar Junction transistor & Field effect Transistor?
   iii. Write any two applications of transistor. (May 09,08)

18. i. With neat diagram explain the various component components in an pnp transistor.
   ii. Explain the input and output characteristics of a transistor in CB configuration. **(May 08, 07, 06)**

19. i. What are the different configurations of BJT?
   ii. Derive the relation between alpha and beta.

iii. Calculate the collector current and emitter current for a transistor with dc = 0.99 and I_{CBO} = 50 μ A when the base current is 20μ A. **(May 07)**

20. Describe a set up to obtain the output characteristics of a transistor in CE configuration. Indicate the various regions of operation on the output characteristics. **(May 07)**

21. i. What is early effect? How does it modify the V-I characteristics of a BJT.
ii. Define alpha and beta of a transistor. Derive the relation between them.
iii. Give reason for cut off conditions for Si and Ge transistors are different. **(May 07)**

22. Describe a set up to obtain the output characteristics of a transistor in CE configuration. Indicate the various regions of operation on the output characteristics. **(May 06)**

23. i. Draw the input characteristics of transistor in CE configuration with regions of operations and explain. Show how h-parameters can be determined graphically. **(Jun 05, Nov, May 03)**
ii. Prove that for a CE transistor in active region $I_C = \beta I_B + (1 + \beta) I_{CO}$ **(Jun 05)**

24. i. Why transistor is considered as current control device. Explain
ii. In a transistor if emitter Junction is forward biased and collector is reverse bias explain its operation.
iii. Explain why alpha < 1and beta > 1for a given transistor **(Jun 05)**

25. i. Explain the operation of NPN and PNP transistors.
ii. Explain the early effect and its consequences. **(Nov 04)**

26. i. Explain active region, saturation region and cuttoff region in transistor characteristics.
ii. Differentiate between NPN and PNP transistors.
iii. Explain the input and output characteristics of the transistor in CC configuration with diagrams. What is the inference from these characteristics. **(Nov 04)**

27. i. Compare CB,CE,CC confgurations with respect to current gain, voltage gain, input resistance and output resistance.
ii. Explain what is meant by Early effect in the case of transistor and what is its consequences. **(Nov 04)**

28. i. Desscribe the two types of breakdown in a transistor.
ii. Why does the CE configuration provide large current amplification while CB does not?
iii. Why is the base of a transistor made thin and is lightly doped? **(Nov 03)**

29. i. Why is CE configuration is most widely used?
ii. Claculate the values of I_C and I_B for a tranisitor with α_{dc}=0.99 and I_{CBO} = 5mA, I_B is measured as 20 mA. **(May 03)**

30. i. Define the following terms and explain.
i. Emitter efficiency
ii. Transport factor
iii. Large signal current gain
ii. The reverse leakge current of the transisitor when connected in CB configuration is 0.2 mA while it is 18 mA when the same transistor is connected in CE configuration. Calculate α_{dc} and α_{ac} of transistor. **(May 03)**

31. Explain the V-I characteristics of UJT? **(May 02)**

32. i.In a common base connection I_E=1mA, I_C=0.95mA, Calculate value of I_B.

ii. In a CB connection, current amplification factor is 0.9. If the emitter current is 1mA. Determine the value of base current. **(May 00)**

33. For a certain transistor collector current is 20mA and current gain factor is 50. Determine emitter current?
In a certain transistor, collector current is 0.98mA and base current is 20mA. Determine the value of
i. Emitter current?
ii. Current amplification factor?
iii. Current gain factor?

(May 00)

34. A silicon transistor with $V_{BE\ (Sat)}$ = 0.2 V is used in the common emitter configuration BJT circuit. Find the minimumvalue of R_C for which the transistor remains in saturation. **(IES'98)**

35. In the transistor circuit shown below I_{CBO} = 2 Amp at 25^0 C and doubles for every 10^0 C increase in temperature. **(IES'97)**

i. Find the maximum allowable value of R_B if the transistor is to remain cut off at 75^0 C. Assume $V_{BE(cut\ off)}$ = -0.1 V.
ii. If V_{BB} = 1.0V and R_B = 50K how high may the temperature increase before the transistor comes out of cut off?

36. A transistor exhibits a change of 0.99 mA in its collector current for a change of 1.0 mA in its emitter current. Calculate its common-base and common-emitter short-circuit current gains. . **(IES'91)**

37. The DC currengain (b) of BJT is 50. Assuming that the emiter injection efficency is 0.995, the base transport factor is:
i. 0.980
ii. 0.985
iii. 0.990
iv. 0.995 **(GATE '07)**

38. Group I lists four diffrerent semiconductor devices. Match each device in Group I with its characteristic property in Group II.

GroupI	GroupII
(P)BJT	(1) Population inversion
(Q) MOS capacitor	(2) Pinch-off voltage
(R) LASER diode	(3) Early effect
(S) JFET	(4) Flat-bandvoltage

i. P-3 Q-1 R-4 S-2
ii. P-1 Q-4 R-3 S-2
iii. P-3 Q-4 R-1 S-2
iv. P-3 Q-2 R-1 S-4 **(GATE '07)**

39. The phenomenon known as —Early Effect"in a bipolar transistor refers to a reductionof the effective base-widthcaused by
i. electron-hole recombination at the base
ii. the reverse biasing of the base-collector junction
iii. the forward biasing of emitter-base junction
iv. the early removal of stored base charge during saturation-to-cutoff switching. **(GATE'06)**

40. A BJT is said to be operated in the saturation region if **(GATE 95)**
   i. both the Junctions are reverse biased
   ii. base-emitter Junction is reverse biased and base –collector Junction is forward biased
   iii. base-emitter Junction is forward biased and base-collector Junction reverse-biased
   iv. both the Junctions are forward biased.

41. If a transistor is operating with both of its Junctions forward biased, but with the collector base forward bias greater than the emitter base forward bias then it is operating in the. **(GATE 95)**
   i. Forward active mode
   ii. Reverse saturation mode
   iii. reverse active mode
   iv. Forward saturation more

UNIT -IV

1. i) Derive the condition for Thermal Stability in a BJT.
   ii) What is meant by Q point of a BJT? What is its significance? **(Nov 13)**

2. i) Write a short note on Miller's Theorem.
   ii) A CB amplifier is driven by a voltage source of internal resistance Rs = 1KΩ. The load impedance is 1KΩ. The transistor parameters are hib = 22Ω, hfb = -0.98, hrb = 2.9x10-4, hob = 0.5μA/V. Compute Ai, Av, Ri, Ro of the amplifier. **(Nov 13)**

3. For the fixed bias configuration determine Ic, Rc, Rb and Vce using following specifications: Vcc=12V; Vc=6v; β=80; Ib=5uA. **(Nov 13)**

4. Find the voltage gain and current gain of a CE amplifier whose hie=1KΩ; hfe=50;

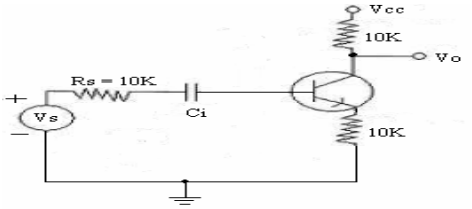
   hre=2.5x10-4 and hoe=25uV. Compute and output impedance of the amplifier? **(Nov 13)**

5. i. With neat diagram and necessary equations, explain how th variations in V_{BE} Compensated with th variations in tmperature.
   ii. Design a slf bias circuit using silicon transistro to achieve a stability factor of 10, with the following specifications; V_{CC} = 16V, V_{BE} = 0.7V; V_{CEO} = 8V, I_{CQ} = 4mA and = 50. **(Dec 12)**

6. i. With neat diagrams and necessary equations, explain the effect of coupling capacitor and bypass capacitor on the performance of an amplifier at lowfrequencis?
   ii. In a single stage CE amplifier circuit, unbypassed emitter resistor, R_C =10K. R_E -1K and R_S - 0.5k. Theh-parametrs of the transistor used are h_{ic} -1.1K, h_{fc} =50, h_{oe} =25 A/V & h_{rc} =2.5X10^{-4}. find R_1 and A_V. **(Dec 12)**

7. i. Draw the circuit diagram & small signal equivalent of CB amplifier using accurate h-parameter model. Derive expressions for AV, AI, Ri and R0.
   ii. Draw small signal equivalent circuit of Emitter Follower using accurate h-parameter model. For the emitter follower circuit with RS = 0.5K and RL = 5K, calculate Ri, AV and RO. Assume, hfe = 50, hie =1K, hoe = 25mA/V. **(Nov 11)**

8. i. In the amplifier circuit shown in Figure.1, estimate input resistance and voltage gain? Also derive the expressions used?



(Nov 11)

ii. Compare CB, CE and CC amplifiers with respect to AV, AI, RI & RO?

9. i. Draw the circuit diagram & small signal equivalent circuit of CE amplifier using accurate h-parameter model. Derive expressions for input resistance and voltage gain?

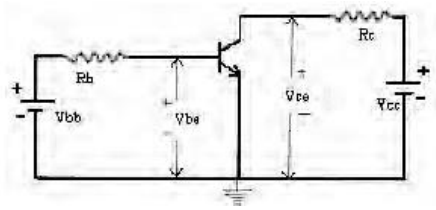
ii. A bipolar junction transistor with hie = 1100□, hfe = 50, hre = $2.4x10^{-4}$, hoe = 25□ A/V, is to drive a load of 1K□ in Emitter-Follower arrangement. Estimate AV, AI, Ri & R0? **(Nov 11)**

10. i. Draw the circuit diagram and small signal model of CE amplifier with unbypassed emitter resistor.. Derive expressions for AV, AI, Ri & R0.

ii. A bipolar junction transistor with hie = 1100□, hfe = 50, hre = $2.4x10^{-4}$, hoe = 25□ A/V, is to drive a load of 1K□ in Emitter-Follower arrangement. Estimate AV, AI, Ri & R0? **(Nov 11)**

11. i. What is 'Thermal Runaway' in transistors? Derive the condition to prevent 'Thermal Runaway' in Bipolar Junction Transistors.

ii. A silicon NPN transistor has Ico = 20nA and □ =150, Vbe = 0.7V. It is operated in Common Emitter configuration (as shown in Figure.1) having Vbb = 4.5V,Rb= 150K,Rc = 3K, Vcc = 12V. Find the emitter, base and collector currents and also verify in which region does the transistor operate. What will happen if the value of the collector resistance is increased to very high values?



(Nov 11)

12. i. What do you mean by biasing a transistor? Explain the need of biasing a transistor for the construction of a faithful amplifier?

ii. Design a collector to base bias circuit using silicon transistor to achieve a stability factor of 20, with the following specifications: VCC = 16V, VBE = 0.7V, VCEQ = 8V, ICQ = 4 mA & β = 50 **(Nov 11)**

13. i. Obtain the condition for thermal stability of a BJT used in a biasing circuit?

ii. Design a self bias circuit using silicon transistor to achieve a stability factor of 10, with the following specifications: VCC = 16V, VBE = 0.7V, VCEQ = 8V, ICQ = 4 mA & β = 5 **(Nov 11)**

14. i. Describe the significance of operating point, DC and AC load lines to ensure active region operation of a BJT in CE amplifier application.

ii. Calculate the Q – point for the DC biased circuit shown below. **(Nov 10)**

15. i. Justify statement "Potential divider bias is the most commonly used biasing method" for BJT circuits. Explain how bias compensation can be done in such biasing through diodes.

ii. An NPN transistor with β = 100 is used in common Emitter configuration with Collector – to – Base bias. If VCC = 10 V, RC = 1 K and VBE = 0 V, determine

a. R_b such that quiescent Collector – to – Emitter Voltage is 4V.

b. The stability factor, 'S'. **(Nov 10)**

16. i. Explain how biasing is provided to a transistor through potential divider bias. List the assumptions made. List the need of bias compensation methods.

ii. An NPN transistor with $\beta = 50$ is used in common Emitter configuration with $V_{CC} = 10V$ and RC = 2.2 K□ . Biasing is done through a 100 KΩ resistance from collector – to – Base. Assuming VBE to be zero volts, Find
a. The quiescent point
b. The stability Factor, 'S'. **(Nov 10)**

17. i. Explain how self biasing can be done in a BJT with relevant sketches and waveforms.
ii. Design a self bias circuit for the following specifications:
VCC = 12 V; VCE = 2V; IC = 4mA; hfe = 80. Assume any other design parameters required. Draw the designed circuit.
(Nov 10)

18. The source and load resistances connected to a BJT amplifier in CE configuration are 680Ω and 1 KΩ respectively. Calculate the voltage gain AV and the input resistance Ri if the h-parameters are listed as h_{ie} = 1.1 kΩ; h_{re} = 2x 10-4, h_{fe} = 50 and h_{oe} = 20 mhos. Compute AV and Ri using both approximate and exact analysis. **(Nov 10)**

19. i. Draw the hybrid equivalent circuit of an NPN. BJT in CE configuration. Derive the expressions for AV, AI, Rin and R_O.
ii. Determine Zi, Zo and AV for the following network for the specifications listed below.
h_{fe} = 110; h_{ie} = 1.1 kΩ; hre = $2x10^{-4}$ and hoe = 20 μA/V **(Nov 10)**

20. i. Explain the concept of biasing for amplification and principle of amplification with a BJT.
ii. For a transistor amplifier, show that the input resistance Ri is given by

$$R_i = \frac{h_i}{(1 - hrAv)}$$

(Nov 10)

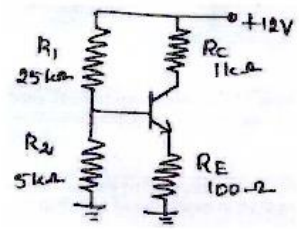
21 i. Draw the low frequency hybrid equivalent circuit for CE & CB amplifier.
ii. Give the approximate h-parameter conversion formulae for CB and CC con-figuration in terms of CE.
iii. Give the advantages of h-parameter analysis.
iv. Give the procedure to form the approximate h - model from exact h - model of amplifier. (May 09, 08)

22. i. Find the value of hfb and hfc, if the value of hfe of a transistor is 50.
ii. A transistor is connected in CC configuration and its h-parameter are hie=1100, hre=2.5 x 10-1, hfe=50, hoe=24mA/V, the circuits uses RL10kand Rs=1k, calculate gain ai. input resistance ri and voltage gain Av of this amplifier. (May 09)

23. Derive the expressions for voltage gain, current gain, I/P impedance, O/P impedance of CE amplifier using exact & approximate model. (May 09)

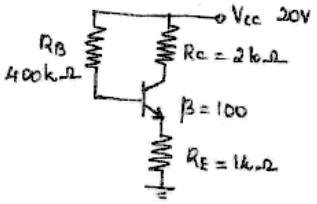
24. i. Write a short notes on millers theorem
ii. Analyse a single transistor amplifier using h-parameters (May 09)

25. i. What is the importance of dc load line?
ii. The figure 5b shows that D.C. bias circuit of a common Emitter trtansistor amplifier. Find the percentage changer in collection curent if the transistor with H_{FE} = 50 is replaced by another transistor with H_{FE} = 150. It is given that the base emitter drop VBE = 0.6V.



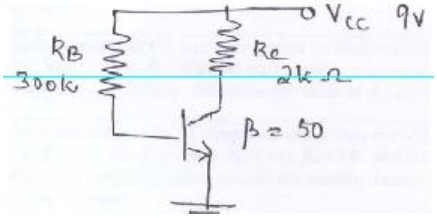
(May 09)

26. i. Explain the criteria for fixing operating point.
    ii. List out the different types of biasing methods. **(May 09,08)**
27. i. Explain the simpler way of drawing dc load line.
    ii. Calculate the dc bias voltage and currents in the circuit shown in figure 5b (Neglect V_{BE} Of Transistor).



(May 09,08)

28. i. Find the collector current and collector to emitter voltage for the given circuit as shown in figuer



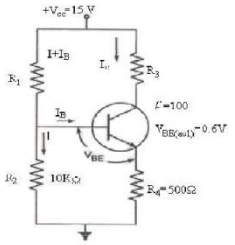
    ii. Can the value of stability factor be less than unity? Explain briefly. (May 09)

29. If the various parameters of a CE amplifier which uses the self bias ethod are V_{CC} = 12 V, *R1* = 10 *k*, R_2 = 5k?, RC 1 *k*, R_e =2 K and = 100, find
    i. The coordinates of the operating point, and
    ii. The stability factor, assuming the transistor to be of silicon. **(May 08)**
30. i. Explain the criteria for fixing operating point.
    ii. List out the different types of biasing methods. **(May 08)**
31. i. Compare A_V, A_i, R_i&R_0 of CE, CB and CC configuration.
    ii. The h-parameters of a transistor used in a CE circuit are h_{ie} = 1.0K, h_{re} = 10x10^{-4}, h_{fe} = 50, h_{oe} = 100 K. The load resistance for the transistor is 1Kin the collector circuit. Determine R_i,R_o,A_V, A_i in the amplifier stage
    (Assume R_s = 1000). **(May 08)**

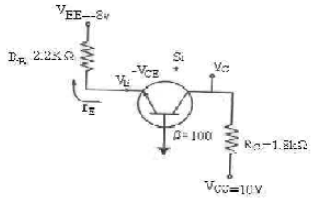
32. i. Draw the circuit diagram of emitter follower circuit using n-p-n transistor and derive expressions for AI ,AV ,Ri,R0 using hybrid model
    ii. Derive expressions for the lower and upper cut off frequencies of an n stage amplifier. **(May 07, Nov 03)**

33. Draw the CE amplifier with unbypassed RE and derive the expressions for voltage gain and current gain. **(May 07)**
34. i. Draw the common base circuit and derive the expressions for voltage gain and current gain.
    ii. Draw the equivalent circuit for CE and CC configurations subject to the restriction that the input is open circuited. Show that the output impedances of the two circuits are identical **(May 07, 06)**
35. i. Explain bias compensation using sensistors.

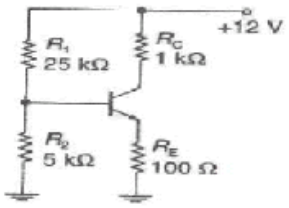
ii. In the circuit shown, if IC=2mA and VCE=3V. Calculate R1 and R3. (figure 5) **(May 07)**



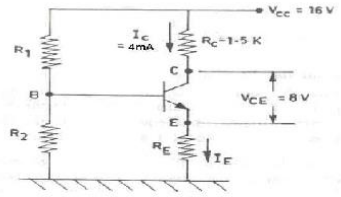
36. i. Explain in detail about thermal runaway and thermal resistance.
    ii. For the circuit shown figure 5b, determine IE, VCand VCE . Assume VBE=0.7V **(May 07)**



37. i. Explain thermal instability. What are the factors affecting the stability factor.
    ii. For the CE amplifier circuit shown below, find the percentage change in collector current if the transistor with h_{fe}=50 is replaced by another transistor with h_{fe}=150. Assume V_{BE}=0.6V **(May 06)**

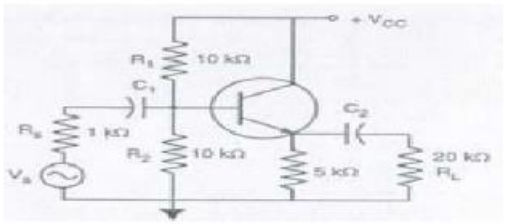


38. i. Draw a BJT self bias circuit and obtain the expression for the stability factor 'S'.
    ii. A Germanium transistor is used in a self biasing circuit configuration as shown below with Vcc = 16V, Rc = 1.5k □ and □= 50. The operating point desired is V_{CE} = 8V and I_C = 4mA. If a stability factor S = 10 is desired, calculate values of R_1, R_2 and R_E of the circuit. **(May 06)**



39. i. Draw a BJT fixed bias circuit and derive the expression for the stability factor 'S'.
    ii. An NPN transistor with □ = 50 is used in a common emitter circuit with V_{CC}= 10V,R_C = 2K ohm. The bias is obtained by connecting a 100K resistance from collector to base. Assume V_{BE} = 0.7 V. Find
    i. the quiescent point and
    ii. the stability factor, S. **(May 06)**
40. Draw a low frequency equivalent circuit for a CC amplifier and derive the relations for the current gain, voltage gain and input resistance in terms of h-parameters. **(May 06)**

41. In the common collector circuit, the transistor parameters are h_{ic}=1.2K□ and h_{fc}= -101. Calculate input and output resistances, voltage gain and current gain.



(May 06)

ii. Draw the h-parameters equivalent circuit of CC, CE configuration and what are the typical values of h-parameters for a transistor in CE and CB configuration. **(Jun 05, Nov 03)**

42. What are the compensation techniques used for V_{BE} and I_{CO}. Explain with the help of suitable circuits. **(Jun 05, Nov 03)**

43. i. What is meant by thermal runway briefly explain?
ii. What is the condition for thermal stability **(May05)**

44. i. Compare common collector and common emitter configuration with regards to R_i, R_o, A_I, A_V.
ii. Draw the circuit diargram of CC amplifier using hybrind parameters and derive expressions for A_I, A_V, R_i, R_o.

(Nov 04, Jun 04)

45. Dertermine A_V, A_I, R_i, R_o from a CE amplifier using npn transistor with hie = 1200Ω, hre = 0, hoe=2 x 10^{-6} mhos. R_L=2.5 kΩ Rs=500 Ω. (neglect the effect of biasing circuit). **(Nov 04)**

46. i. Draw the circuit diagram of a collector to base bias circuit of CE amplifier and derive expression for S.
ii. Determine the quiescent currents and the collector to emitter voltage for a germanium transistor β=50 in self biasing arrangement. Draw the circuit with a given component value V_{CC}=20V, R_C=2KΩ, R_e=100Ω R_2=5KΩ. Also find out stability factor.
(May05, Jun 04)

47. i. Define the stability factors S', S'' and what is the need of this in BJT circuits.
ii. Draw the circuit diagram of a self bias BJT circuit and explain how to determine the values of R_1 and R_2. **(Nov 04)**

48. i. What is meant by thermal runaway? Breifly explain?
ii. What is the condition for thermal stability?
iii. An n-p-n transistor if □=50 is used in common emitter circuit with V_{cc} = 10v and R_c = 2k . the bias is obtained by connecting 100k□ resistance from collection to base. find the quiescent point and stability factor S. **(Nov 04, May 03)**

49. i. Draw the circuit diagram of a self bias circuit and derive expression for S. why it is widely used?
ii. How to obtain quiescent point graphically for a given transistor amplifier of CE configuration?
iii. How to obtain quiescent point graphically for a given transistor amplifier of CE configuration? Explain. **(Nov' 04, May' 03)**

50. i.Draw the circuit diagram of fixed bias circuit in CE configuration and obtain the expression for I_B. Why the ciruit is not suitable if the Beta of the transistor is changed.

ii. How to obtain bias stability in CE configuration circuit.

iii. Briefly explain about thermal stability. **(Nov'03)**

51. i. Draw the circuit diagramof small signal CE amplifier circuit and give its equivalent hybrid model. What is the role of CC and Ce.

ii. Obtain frequency response of CE amplifier circuit and find out its band width. What is the impact of Co and Cs on the band width. **(May 03)**

52. In self biased CE amplifier R_c=4kΩ, R_1=90kΩ, R_2=10kΩ, β=45 and V_{BE}=0.6V. Compute the stability factor S for the following values of R_e

i. 1kΩ
ii. 1.5kΩ
iii. 1.8kΩ **(Dec'03)**

53. For the CE self bias circuit R_e=2kΩ, R_b=8kΩ. The collector supply voltage V_{cc} and R_e are so adjusted that the collector current I_c at 25^{o}C is 2mA. Determine variation of I_c over the temperature range of -65^{o}C to +75^{o}C for a Germanium transistor using typical values of V_{BE} and β. **(May'02)**

54. In the self biased CE amplifier R_e=5kΩ, R_2=9kΩ, R_1=81kΩ, β=50 and R_c=810kΩ. Compute the stability factor S. **(Nov'02)**

55. In the CE amplifier self bias R_1=90kΩ, R_2=10kΩ, R_e=2kΩ and α=0.99. According to the manufacturer's data, collector reverse saturation current I_{co} varies from 5 to 30mA over the working temperature range. Find the variation in the collector current I_c when

i. Amplifier is unstabilized
ii. Stabilizing resistor R_e is used. **(May'02)**

56. A germanium transistor is used in the self-biasing arrangement. Given V_{cc}=16V and R_c=1.5Kohm. The quiescent point is chosen to be V_{CE}=8V and I_c=4mA. A stability factor=12 is desired. If □=50 find the resistance values of R_1, R_2 and R_e. **(Nov'02)**

57. Explain the terms bias stabilization and bias compensation? **(Nov'02)**
Draw the circuits and explain the principles of working of Diode compensation for V_{BE} and I_{CO}?

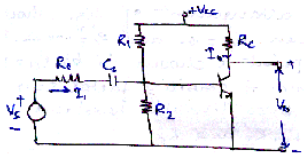
58. The beta of a transistor is 49 and its Ic varies from 0.1 to 20 Nano Amperes when the temperature changes from 25^{o}C to 100^{o}C. Calculate the stability factor and the corresponding change in the collector current if the voltage divider bias is used. **(Nov'02)**

59. In the biasing feedback resistor method a Si transistor with feedback resistor is used the operating point is 7V and I_C=1mA. Vcc=12V, Assume beta=100 determine the value of R_B and stability factor

(Nov' 02)

60. What is thermal-runaway? Derive a condition for preventing thermal runaway in a self-biased BJT?
For a transistor amplifier shown in figure below: calculate **(Nov 02)**

i. $A_I=I_o/I_i$
ii. A_v
iii. R_o and R_i



61. A Junction transistor has the following h-parameters h_{ie}=2000Ω, h_{re}=1.6x10^{-4} h_{fe}=49, h_{oe}=50mA/V. 7Determine the current gain, voltage gain, input resistance and output resistance of the CE amplifier if the load resistance is 30KΩ and the source resistance is 600Ω? **(Nov 02)**

62. Draw the dc and ac load lines for the CE circuit shown below. What is the maximum peak-to-peak signal that can be obtained? **(Dec 02)**

63. In a transistor amplifier, change of 0.025V in signal voltage causes base current to change by 15mA and collector current by 1.2mA. If collector and load resistances are of 6KΩ and 12KΩ, determine

i. Input resistance
ii. Current gain
iii. AC load
iv. Voltage gain
v. Power gain

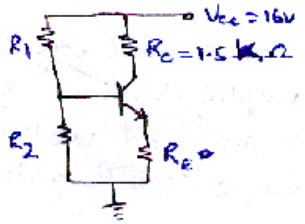
(Jun 02)

64. For a fixed bias arrangement Vcc=12V, and the DC bias conditions are Vce=2V; hFE=80 and Ic=4mA. Calculate R_c and R_b **(May 01)**

65. The CE self biased amplifier uses npn transistor having β=100, I_{co}=1mA, R_1=90kΩ, R_2=10kΩ, V_{cc}=+12V, R_e=100Ω and R_c=1kΩ. The quiescent collector current I_c=4mA. Find the value of stability factor S and the largest value of thermal resistance which permits thermally stable circuit. **(Nov 01)**

66. An npn transistor used in the self bias CE amplifier has a value of β =49 at temperature of 25^{o}C. The circuit has R_1=90k Ω, R_2=10k Ω and R_e=1k Ω. V_{cc} and R_c are adjusted to establish I_c equal to 2mA. Calculate the values of stability factors. **(Jun 01)**

67. Calculate the dc bais voltages and currents for the self bias currents for the self bias circuit V_{CC}=12V, R_1=40k Ω, R_2=5k Ω, R_C=5k Ω, R_e=1k Ω. Assume V_{BE}=0.3V, β =60 for the transistor used.



(Nov 01)

68. Draw the h-parameters equivalent circuit for transistor amplifier in the three configurations? What are the limitations of h-parameters? **(May 01)**

69. Discuss the transistor amplifier characteristics in common emitter configuration and their variation with R_S and R_L with the help of equation? **(Nov 01)**

70. Analyze CE, CC and CB amplifiers using the approximate hybrid model **(Nov 01)**

. A BJT has h_{ie}=2K Ω, h_{fe}=100, h_{re}=2.5x10^{-4} and h_{oe}=25μA/V as parameters in CE configuration, It is used as an emitter follower amplifier with R_S=1K Ω and R_L=500 Ω. Determine for the amplifier

i. Voltage gain $A_{vs}=V_o/V_s$
ii. Current gain $Ais=I_o/I_o$
iii. Input resistant R_i
iv. Output resistance R_o **(Nov 00)**

71. The following test results were obtained in a CE amplifier circuit while measuring h-parameters experimentally. **(Nov 00)**

i. With AC output shorted, I_b=20mA, I_c=1mA, V_{be}=22mV and V_{ce}=0.
ii. With AC output open-circuited I_b=0, V_{be}=0.25mV, I_c=30 μ A and V_{ce}=1V.

Determine hybrid parameters of the given transistor.

72. Explain why bias stabilization is done in the bipolar Junction transistor amplifier circuit. **(IES'01)**

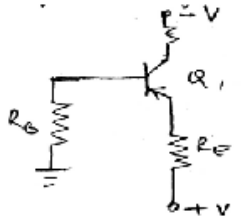
73. Draw a fixed bias circuit and a self bias circuit using a BJT and mention typical component values and supply voltages for these circuit. **(IES'01)**

74. Briefly explain the principle of operation of fixed bias and self bias circuits using BJT. **(IES'01)**

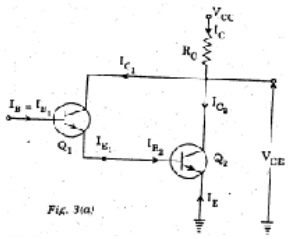
75. Compare the relative merits and demerits of fixed bias and self bias circuits using BJT from the application point of view, choose with suitable reasons, the one which you would recommend for cascade amplifier operation. **(IES'01)**

76. Derive an expression for the stability factor of the self bias circuit of BJT **(IES'00)**

77. Derive an expression for the stability factor of the circuit shown below **(IES'00)**

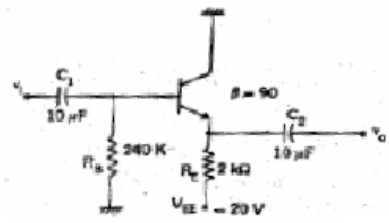


78. For the circuit shown in Fig.3i., $_1$ = 0.98, $_2$ = 0.96, V_{cc} = 24, R_c = 120 and I_E = - 100 mA. Calculate the currents I_{C1}, I_{B1}, I_{E1}, I_{B2}, I_{C2} and I_C, the voltage V_{CE} and the ratios I_c / I_B and I_c / I_E, Neglect reverse saturation currents. **(IES'98)**

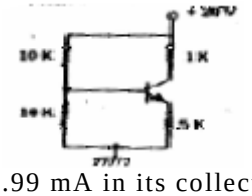


79. A silicon transistor with $V_{BE(Sat)}$ = 0.2 V is used in the common emitter configuration BJT circuit. Find the minimum value of R_C for which the transistor remains in saturation. **(IES'98)**

80. Determine V_{CE} and I_E for the following network. **(IES'96)**

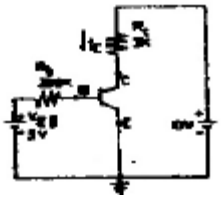


81. Calculate the emitter current in the voltage divider bias circuit shown. What is the value of V_{CE} and V_C ? make reasonable assumptions. **(IES'93)**

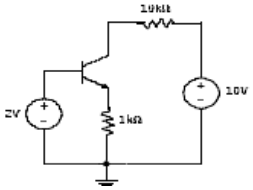


82. A transistor exhibits a change of 0.99 mA in its collector current for a change of 1.0 mA in its emitter current. Calculate its common-base and common-emitter short-circuit current gains (vcc=20v**)**. **(IES'91)**

83. Find the transistor currents in the circuit shown below A silicon transistor with □ = 100, I_{C0} = 20 nA is under consideration. **(IES'90)**



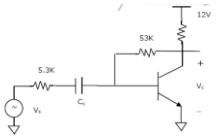
84. For the BJT circuit shown, assume that the □□ of the transistor is very large and V_{BE}=0.7*V*. The mode of operation of the BJT is



i. cut-off
ii. saturation
iii. normal active

iv. reverse active

85. CommonDatafor Questions 71, 72, 73:
In the transistor amplifier circuit shown in the figure below, the transistor has the following parameters:
b_{DC} =60,V_{BE} =0.7V, h_{ie} and h_{fe} tends to infinty The capacitance C_c canbe assumed infinty



(GATE'06)

86. Under the DC conditions, the collector-to-emitter voltage drop is:
i. 4.8 Volts
ii. 5.3 Volts
iii. 6.0 Volts
iv. 6.6 Volts

87. If Beta$_{DC}$ is increased by 10%, the collector-to-emitter voltage drop
i. increases by less than or equal to 10%
ii decreases by less than or equal to 10%
iii. increases by more than 10%
iv. decreases by more than 10%

88. Explain and draw the capacitance vs gate voltage (C-V $_g$**)** characteristic of a Si NMOS device at i. low and ii. high frequencies. What parameters can be determined from these characteristics? **(IES'02)**

89. For the common emitter amplifier draw the simplified high frequency equivalent circuit and derive an approximate expression for the voltage gain and 3 dB frequency.
(IES'00)

90. Design a Junction FET amplifier to operate from 12 V supply with a gain of at least 5 Bias at V_{DQ} =0.25 mA, Y_{GSQ} = -0.6V Estimate R_D, R_s, g_m and voltage gain A choose R_G = 1M, C_1=C_2= mF, Estimate C_s to work satisfactorily for f=1000H$_z$. **(IES'91)**

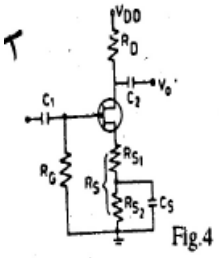
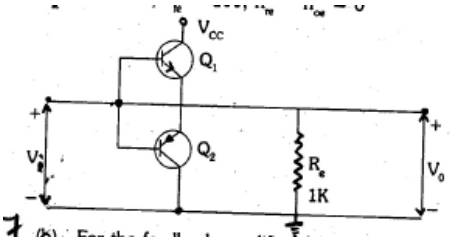


Fig.4

2N 3438
$V_{GS(OFF)} = V_p = -2$ V
$I_{DSS} = 0{\cdot}5$ mA
$BV_{GSS} = 50$ V
$I_{G(OFF)_{max}} = 0{\cdot}5$ mA

Also prove $$g_m = -\frac{2I_{DSS}}{V_P}\left[1-\frac{V_{GS}}{V^P}\right]$$

91. Derive the expressions for the voltage gain A_v and the input resistance R_{in} of the amplifier shown. Find the values of A_v and R_{in} for the following values of h parameters for the transistors.
h_{ie} = 1000□, h_{fe} = 100, h_{re} = h_{oe} = 0 **(IES'97)**



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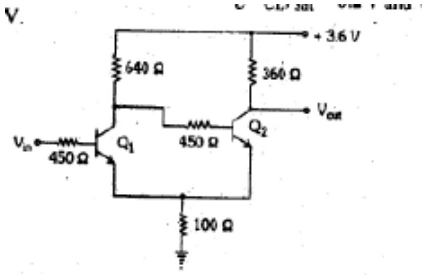
92. For the transistor circuit shown below, determine the voltage transfer characteristic, assuming
$V_{CE, sat}$ = 0.2 V and V_{BE} on = 0.7 V. **(IES'96)**



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93. For the network determine the following parameters using the complete hybrid equivalent model and
compare with the results obtained using the approximate model in which the effects of h_{re} and h_{oc} are neglected.
(IES'96)
The h-parameters of the transistor are
i. Z_i and Z'_i
ii. A_V
iii. $A_i=I_0 / I_i$ and A'_i
iv. Z_o
the h-parameters of the transistor are:h_{fe} = 110, h_{ie} = 1.6 K h_{re} = 2 x 10 10^{-4}, h_{oe} = 20

94. A cascade amplifier stage is equivalent to **(GATE'97)**
i. a common emitter stage followed by a common base stage
ii. a common base stage followed by a common base stage
iii. an emitter follower stage followed by a common base stage
iv. a common base stage followed by a common emitter stage

95. In a common emitter BJT amplifier, the maximum usable supply voltage is limited by **(GATE'97)**
i. Avalanche breakdown of Base-Emitter Junction
ii. Collector-Base breakdown voltage with emitter open (BV_{CBO})
iii. Collector-Emitter breakdown voltage with base open (BV_{CBO})
iv. Zener breakdown voltage of the Emitter-Base Junction.

96. An npn transistor has a beta cutoff frequency $f_{\square\square}$ of 1 MHz, and common emitter short circuit low-frequency current gain $\square_0$ of 200. its unity gain frequency f_T and the alpha cutoff frequency $f_{\square\square}$ respectively are **(GATE'96)**
i. 200 MHz, 201 MHz
ii. 200 MHz, 199 MHz
iii. 199 MHz, 200 MHz
iv. 201 MHz, 200 MHz

97. Match the following

i. Cascade amplifier	1) does not provide current gain
ii. Differential amplifier	2) is a wideband amplifier
iii. Darlington pair common emitter amplifier	3) has very low input impedance and very high current gain
	4) has very high input impedance and very high current gain
	5) Provides high common mode voltage rejection.

(GATE'96)

98. An RC-coupled amplifier is assumed to have a single pole low frequency transfer function. The maximum lower cut-off frequency allowed for the amplifier to pass 50 Hz square wave with no more maximum lower cut-off frequency allowed for the amplifier to pass 50 Hz square wave with no more than 10% tilt is _____ **(GATE 95)**

99. The f_T of a BJT is related to its g_m, $C\mu$ and C as follows: **(GATE'98)**

i. $f_T = \dfrac{C_\pi + C_\mu}{g_m}$

ii. $f_T = \dfrac{e\pi(C_\pi + C_\mu)}{g_m}$

UNIT-V

1. i) Explain construction and working of an n channel JFET with neat diagram and symbol.
   ii) Define the parameters of JFET and derive the relation between them. **(Nov 13)**

2. i) With the help of neat diagram Explain the voltage divider biasing method for FET.
   ii) Compare important characteristics of JFET and MOSFET. **(Nov 13)**

3. i) Draw the static and drain characteristics and the transfer characteristic curves for N-channel enhancement type MOSFET. **(Nov 13)**

4. Explain the voltage divider biasing of JFET and also derive the necessary equations. **(Nov 13)**

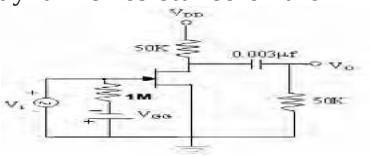
5. i. Draw the basic structure and circuit arrangemnt of a p=chammel Metal oxide Semiconductor Field Effect Transistor in enhancement mode. Explain the drain and transfer characteristies.
   ii. Explain the procedure to obtain the small -signal equivalent circuit of a field effect transistror wiht necessary equations. Also draw th small -signal model. **(Dec 12)**

6. i. What are the rquirments of FET biasing? Verify these requirments in source slf -bias circuit.

ii. A Common Source FET amplifier Circuit shown in Figure .3 with unbypassed R_S has the following circuit parameters: =15K. R_S =2.5K, R_g= 1M, r_d = 100K, I_{DSS} =10mA, VP = 5V andV_{DD} =20V. Calculate g_m &A_V

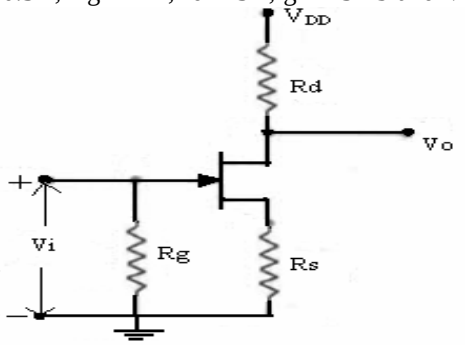
(Dec12)

7. i. Show the self-bias arrangement for a Field Effect Transistor. With necessary expressions describe the procedure of Q-point establishment and stabilization?
   ii. In the common source FET amplifier shown in Figure.2, the transconductance and drain dynamic resistance of the FET are 5mA/V and 1MW respectively. Estimate AV, Ri & R0.



(Nov 11)

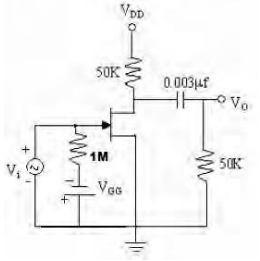
8. i. Explain the need of biasing a Field Effect Transistor. With necessary equations and valid reasons explain why a simple 'fixed bias' arrangement for FETs is not used in practical applications?
   ii. A Common Source FET amplifier circuit shown in Figure.2 with un-bypassed RS has the following circuit parameters: Rd = 15K, RS = 0.5K, Rg = 1M, rd = 5K, gm= 5mS and VDD = 20 V. Calculate AV, AI, Ri and R0.



(Nov 11)

9. i. Draw the basic circuit and small-signal model of Common Drain FET amplifier. Derive expressions for voltage gain and output resistance?
   ii. Compare the merits & demerits of a Bipolar Junction Transistor (BJT) with Field effect Transistor (FET) in detail? **(Nov 11)**

10. i. Draw the basic structure and equivalent circuit of UJT. Explain how the UJT can be used as a negative-resistance device with the aid of static characteristics.
    ii. In the common source FET amplifier shown in Figure.1, the transconductance and drain dynamic resistance of the FET are 5mA/V and 1MÙ respectively. Estimate AV, Ri & R0?



(Nov 11)

11. i. With the help of neat sketches and characteristic curves explain the construction & operation of a JFET and mark the regions of operation on the characteristics?
    ii. Show that in Field Effect Transistor, the transconductance, gm = gmo [1- VGS/ Vp] **(Nov 11)**

12. i. Explain the construction & operation of a P-channel MOSFET in enhancement and depletion modes with the help of static drain characteristics and transfer characteristics?

ii. In an n-channel FET, the effective channel width is 3x 10-4cm and the donor impurity concentration is 1015 electrons/cm3. Find the pinch-off voltage? **(Nov 11)**

13. i. Explain the construction & operation of a N-channel MOSFET in enhancement and depletion modes with the help of static drain characteristics and transfer characteristics?

ii. In an n-channel FET, the effective channel width is 3x 10^{-4}cm and the donor impurity concentration is 1015 electrons/cm3. Find the pinch-off voltage? **(Nov 11)**

14. i. Explain the construction & operation of a P-channel MOSFET in enhancement and depletion modes with the help of static drain characteristics and transfer characteristics?

ii. "A depletion mode MOSFET can also be operated in enhancement mode but an enhancement mode MOSFET cannot be operated in depletion mode". Justify? **(Nov 11)**

15. i. Draw the symbol and equivalent circuit of a UJT. Explain the operation of UJT with the help of its V – I characteristics.

ii. With the help of relevant schematic, explain the functioning of a common amplifier. **(Nov 10)**

16. i. Detail the construction of an n-channel MOSFET of depletion type. Draw and explain its characteristics.

ii. A self biased p – channel JFET has a pinch – off voltage of VP = 5 V and IDSS = 12 mA. The supply voltage is 12 V. Determine the values of RD and RS so that ID = 5 mA and VDS = 6V **(Nov 10)**

17. i Explain the significance of threshold voltage of a MOSFET. Discuss the methods to reduce threshold voltage, VT.

ii. A FET follows the relation $I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$ What are the values of ID and gm for VGS = -1.5 V if IDSS and VP are given as 8.4 mA and -3V respectively. **(Nov 10)**

18. i. Explain how a FET can be made to act as a switch.

ii. Show that the transconductance, gm and drain current, IDS of a FET are related through

Define other terms of the equation.

iii. List any four merits of MOSFET to show that they are more suitable than JFETS in Integrated circuits. **(Nov 10)**

19. i. Differentiate between enhancement and depletion modes of a MOSFET with the help of its characteristics and construction.

ii. Determine the pinch off voltage for an N . channel silicon. JFET if the thickness of its gate region is given as 3.2x10^{-4} cm and the donor density in n-type region is 1.2 x10^5/cm^3.

$$g_m = \frac{2}{|V_P|}\sqrt{I_{DSS}\ I_{DS}}$$

iii. Establish a relation between the three JFET parameters, □, rd and gm. **(Nov 10)**

20. i. With a neat schematic, explain how amplification takes place in a common drain amplifier.

ii. Describe the application of a UJT as a relaxation oscillator. **(Nov 10)**

21. i. With the help of a neat schematic, explain the functioning of a common source amplifier.

ii. Bring out the differences between BJT and FET. Compare the three configurations of JFET amplifiers. **(Nov 10)**

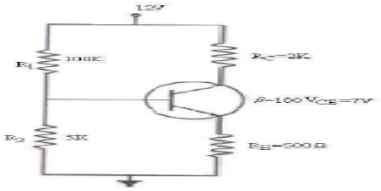
22. i. Describe how a FET can be used as a voltage variable Resistance (VVR).

ii. With the help of circuit diagram and its equivalent circuit of a source follower, derive an expression for the voltage gain possible. **(Nov 10)**

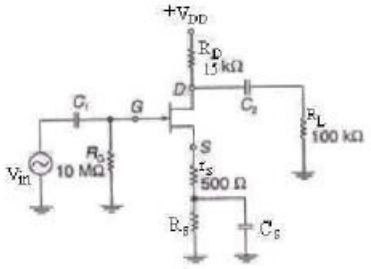
23. i. How the UJT differs from ordinary PN diode.
ii. Explain the construction of UJT.
iii. Draw and explain the equivalent circuit of UJT. **(May 08)**

24. i. What are the biasing schemes available to achieve the required bias in a Junction field effect transistor. Explain any one of the biasing schemes.
ii. For the circuit shown figure 5b, Find the values of VDS and VGS. Given ID=5mA, **(May 07)**

$V_{DD}=10V$, $R_D=1K\Omega$, $R_S=500\Omega$

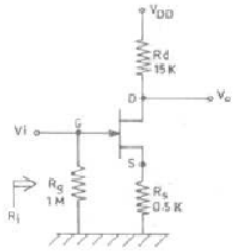


25. The figure is a swamped FET amplifier. Determine the voltage gain when RL=100K. Neglect the FET output resistance (rd) Take gm = 4 mS.



(May 07)

26. A common source FET amplifier circuit shown in with unbypassed R_S has the following circuit parameters: R_d = 15k, R_s = 0.5k, R_g = 1M, r_d = 5k, g_m= 5 m mho and V_{DD} = 20 V. Calculate A_V and R_O



(May 07, 06)

27. Explain the principle of MOSFET in depletion mode. With neat sketches and o/p characteristics. **(May 07)**

28. i. Define the different parameters of FET.
ii. What are special semiconductor devices? Give explanation for any two devices. **(May 07)**

29. Explain the principle of MOSFET in depletion mode, with neat sketches and o/p characteristics. **(May 06)**
30. Draw the circuit diagram of common drain amplifier and derive expressions for voltage gain and input resistance. **(May 06)**

31. i. Draw the circuit diagram of common drain amplifier and derive expressions for voltage gain and output resistance.
ii. Draw the equivalent circuits for CE and CC configurations subject to the restriction that R_L=0. Show that the input impedances for the two circuits are identical. **(May 06)**

32. Compare JFET and MOSFET with respect to various features **(May05)**

33. i Discuss the static drain and gate characteristics of an N-channel enhancement type MOSFET?

ii. Draw the biasing circuit suitable for JFET and if the JFET is replaced by a MOSFET for what mode of operation it is valid and explain about the function of each component used in the circuit. **(May05)**

34. When a reverse gate voltage of 12V is applied to JFET, the gate current is 1mA. Determine the resistance between gate and source. **(Dec 04)**

35. i. Sketch the cross section of an NMOS enhancement transistor and briefly explain.
ii. What is the significance of the threshold voltage V_T in i. enhancement mode ii. depletion mode MOSFETS.
iii. Define Rd, g_m and μ of JFET. **(Nov 04)**

36. i. For a MOSFET if V_{GS} varies from negative to positive voltage. Draw the transfer characteristic and mention modes of operation.
ii. Sketch the drain characteristicsts of MOSFET for different values of V_{GS} and mark different region of operation. **(Nov 04, May 03)**

37. i. Explain how FET works as voltage variable resistor?
ii. Explain the constructional features of a depletion mode MOSFET and explain its basic operation.

(Nov 03)

38. i. Give symbol of UJT and mark required polarites for operation.
ii. Give the equivalent circuit and UJT.
iii. Explain how the UJT can be treated as a negative resistance device with the aid of static characteristic.

(May 03)

39. A JFET has the following parameters I_{DSS}=5mA, V_D=2V. In a self bias N-channel JFET the operating point is to be set at I_D=1.5mA and V_{DS}=10V and V_{DD}=20V. Find the value of R_S and R_D and the resistance to be connected between source and ground. **(May 01)**

40. A transistor used in the amplifier circuit show in the following h-parameters:
h_{fe} =100 □, h_{oe} =50 X10^{-6} □$^{-1}$ and h_{fe} =55
Calculate the voltage and power gains of the circuit. Find also percentage error in the values obtained h_{oe} is neglected. **(IES'93)**

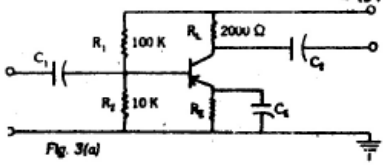


Fig. 3(a)

41. For the JFET amplifier in common source configuration the values in the circuit are I_{DSS} = 5mA; V_{PO} = 3V with usual notations. Also in this circuit
R_D = 2K □ : R_S = 8K □ , V_{DD} = 15 V; V_G =10 V;
And V_{ss} = -8 V. Calculate V_{GS} and V_o **(IES'94)**

42. An n-channel JFET has I_{DSS} = 1 mA and V_P = -5 V. Its maximum Transconductance is _____
(GATE 95)

43. With a sketch of characteristics, explain the features of a power MOSFET **(IES'00)**

44. A JFET with the following parameters is used in a single stage common source amplifier with a load resistance of 100 K□. Calculate the high frequency cut off (upper 3 dB cut off frequency**)** of the amplifier. **(GATE'93)**
g_m = 2.0 m A/V
C_{gd} = 2.0 p.F
C_{rd} = 100
C_{gd} = 2.5 pF
C_{gd} = 1.0 pF

EDC
Assignment –I

1. Sketch V-I characteristics of a PN diode for the following conditions:
   i. R_f=0, V= 0, R_r =∞
   ii. R_f = o, V=o.6V, Rr = ∞
   iii. R_f = Non -zero , fixed value, V= 0, R_r=∞
   iv. R_f= Non -zero ,fixed value, V= 0.6V, R_r = ∞
   Where V is the cut -in voltage, R_f is the forward dynamic resistance & R_r is the reverse dynamic resistance of the diode.

2 Derive the expression for transition capacitance, CT of a PN diode.

3 With the help of V-I Characteristics, explain the operation of a PN Diode under Forward bias and Reverse bias.

4. i. Explain the process of break down of a p-n Junction diode due to
   a. Avalanche effect b.Zener effect

5. i.Define the following terms for a PN diode
   a) Dynamic resistance b) Load line
   c) Difference capacitance d) Reverse saturation current

6. Explain the temperature dependence of VI characteristics.

7. Explain the operation of Tunnel diode.
8. Explain the operation of Varactor Diode.
9. Explain the operation of Silicon Controlled Rectifier.
10. Explain the operation of Photo diode.

Assignment –II

1 Draw the block diagram of a regulated power supply and explain its operation. Explain the operation of Zener Voltage Regulator using Zener diode.

2 A full wave bridge rectifier having load resistance of 100 is fed with 220V, 50Hz through a step-down transformer of turns ratio 11:1. Assuming the diodes ideal, find
   a. DC output voltage
   b. Peak inverse voltage
   c. Rectifier efficiency.

3 With neat sketches explain the operation of a FWR with L- section filter & derive the expression for itsripple factor. Also explain the necessity of a bleeder resistor in a practical L- section filter.

4 Determine the ripple factor of an L-section filter comprising a 10H choke and 8F capacitor, used with a FWR. The DC voltage at the load is 50V. Assume the line frequency as 50Hz.

5. What is the ripple factor if a power supply of 220 V, 50 Hz is to be Full Wave rectified and filtered with a 220 F capacitor before delivering to a resistive load of 120 ? Compute the value of the capacitor for the ripple factor to be less than 15%.

6. Derive expressions for ripple factor of a Full Wave Rectifier with a capacitive filter and inductive filter.

7. Compute the average and RMS load currents, TUF of an unfiltered centre tapped Full Wave Rectifier specified below.
   Input voltage to transformer = 220 V/50 Hz.
   Step down ratio of centre tapped transformer = 4:1(Primary to each section secondary).
   Sum of transformer secondary winding in each secondary segment and diode forward resistance = 100 □.
   Load resistance, R_L = 220 □.

8. List out the merits and demerits of Bridge type Full Wave rectifiers over centre tapped type Full Wave rectifiers.

9. The secondary voltages of a centre tapped transformer are given as 60V-0V-60V the total resistance of secondary coil and forward diode resistance of each section of transformer secondary is 62□. Compute the following for a load resistance of 1 K□.
   a) Average load current
   b) Percentage load regulation
   c) Rectification efficiency
   d) Ripple factor for 240 V/50Hz supply to primary of transformer.
   e) What is bleeder resistance in L – section filters?

Assignment-III

1. Draw the circuit diagram of NPN transistor in Common Base (CB) configuration. With neat sketches and necessary equations, describe its static input- output characteristics and clearly indicate the cut-off, saturation & active regions on the output characteristics?

2. With necessary diagram explain the input and output characteristics of common-emitter configuration.

3. What is Early-effect; explain why it is called as base-width modulation? Discuss its consequences in transistors in detail?

4. Derive the relationship among α, β and γ of a transistor. Derive the relation between them.

5. With a neat diagram explain the various current components in an NPN bipolar junction transistor & hence derive general equation for collector current, IC?

6. Calculate the values of I_C and I_E for a transistor with $\alpha_{dc} = 0.99$ and $I_{CBO} = 5$ μ A, if IB is measured as 20μ A.

7. The reverse leakage current of the transistor when connected in CB configuration is 0.2μA and it is 18μA when the same transistor is connected in CE configuration. Calculate α_{dc} and β_{dc} of the transistor. Assume necessary values.

8. With reference to a BJT, define the following terms and explain:

   i) Emitter efficiency.
   ii) Base transportation factor.
   iii) Large signal current gain.

9. Prove that for a CE transistor in active region $IC = \beta IB + (1 + \beta)I_{CO}$.

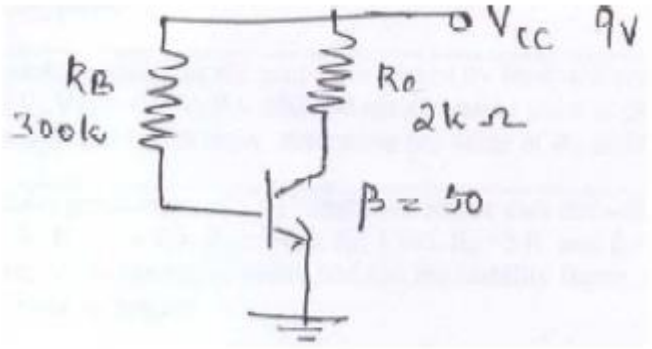
10. 4. Compare CB, CE and CC amplifiers with respect to AV, AI, RI & RO?

Assignment-IV

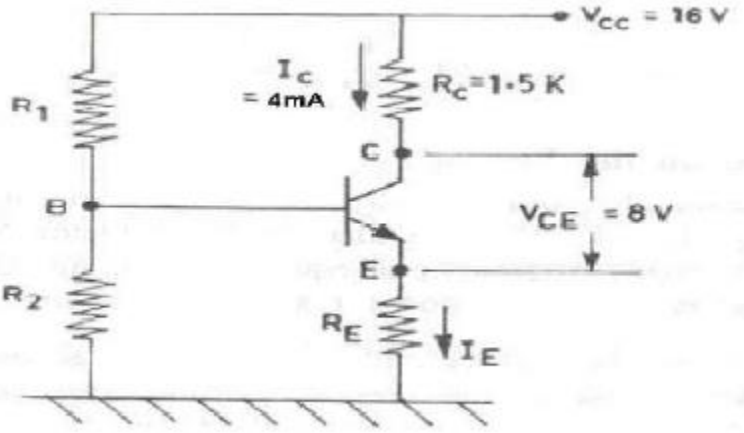
1. Draw a fixed circuit and derive an expression for the stability factor?

2. Design a collector to base bias circuit using silicon transistor to achieve a stability factor of 20, with the following specifications: VCC = 16V, VBE = 0.7V, VCEQ = 8V, ICQ = 4 mA & β = 50.

3. Describe the significance of operating point, DC and AC load lines to ensure active region operation of a BJT in CE amplifier application.
4. Find the collector current and collector to emitter voltage for the given circuit as shown in figure.



5. A Germanium transistor is used in a self biasing circuit configuration as shown below with Vcc = 16V, Rc= 1.5kΩ and β= 50. The operating point desired is V_{CE} = 8V and IC = 4mA. If a stability factor S = 10 is desired, calculate values of R1, R2 and RE of the circuit.



6. Draw a BJT self bias circuit and obtain the expression for the stability factor S,S',S''.

7. In a single stage CE amplifier circuit, unbypassed emitter resistor, RC =10K. RE -1K and RS - 0.5k. The h-parameters of the transistor used are hic =1.1K, hfc =50, hoe =25 Ω A/V & hrc =2.5X10-4. find R1 and AV.

8. Draw the circuit diagram & small signal equivalent of CB amplifier using accurate h-parameter model. Derive expressions for AV, AI, Ri and R0.
9. i. Define all the four hybrid parameters of a BJT in CE configuration. Draw the circuit and its equivalent circuit.
   ii. The source and load resistances connected to a BJT amplifier in CE configuration are 680Ω and 1 KΩ

   respectively. Calculate the voltage gain AV and the input resistance Ri if the h-parameters are listed as hie = 1.1 kΩ; hre = 2x 10-4, hfe = 50 and hoe = 20 μmhos. Compute AV and Ri using both approximate and exact analysis.

10. Analyze the CC amplifier using Approximate analysis ad find Av,Ai,Ri,Ro,Avs and Avs.

Assignment-V

1. Explain the principle of Operation and VI-characteristics of JFET.
2. Derive the expression for Pinch-off Voltage.
3. Explain JFET small-signal Model.
4. Expian the principle of operation of Enhancement MOSFET.
5. Comapre MOSFET with JFET.
6. Explain the operation FET CS Amplifier.
7. Explain the operation FET CD Amplifier.
8. Compare BJT and FET.
9. Explain UJT VI-Characteristics.